UC.2000 : 8 bit A/D Digitizers, up to 200 MS/s

- **CompactPCI 6U format**
- **Up to 200 MS/s on 2 channels**
- **Up to 100 MS/s on 4 channels**
- **Simultaneous sampling on all channels**
- **7 input ranges: ±50 mV up to ± 5 V**
- **Up to 512 MSample memory**
- **FIFO mode for slower sampling rates**
- **Window and pulsewidth trigger**
- **Input offset up to ±400%**
- **Multiple card synchronization option**
- **Windows program SBench 5.x included**

Product range overview

The UltraFast CompactPCI cards are based on more than 16 years design experience. The cards are high-quality, low-noise PC-based instruments that have deeper memory and more flexibility than traditional oscilloscopes.

Model	1 channel	2 channels	4 channels
UC.2020	50 MS/s	50 MS/s	
UC.2021	50 MS/s	50 MS/s	50 MS/s
UC.2030	200 MS/s	100 MS/s	
UC.2031	200 MS/s	200 MS/s	100 MS/s

Software/Drivers

A large number of drivers and examples are delivered with the board or are available as an option:

- Windows 98/ME/NT/2000/XP - drivers
- Linux - drivers
- SBench 5.2
- Streaming Software SPviewIT 6.2 (as option)
- Visual C++/Borland C++ Builder examples
- Borland Delphi examples
- Microsoft Visual Basic examples
- Microsoft Excel examples
- LabWindows/CVI examples
- FlexPro support with SBench
- LabVIEW - drivers (as option)
- DASYLab - drivers (as option)
- MATLAB - drivers (as option)
- Agilent VEE - drivers (as option)

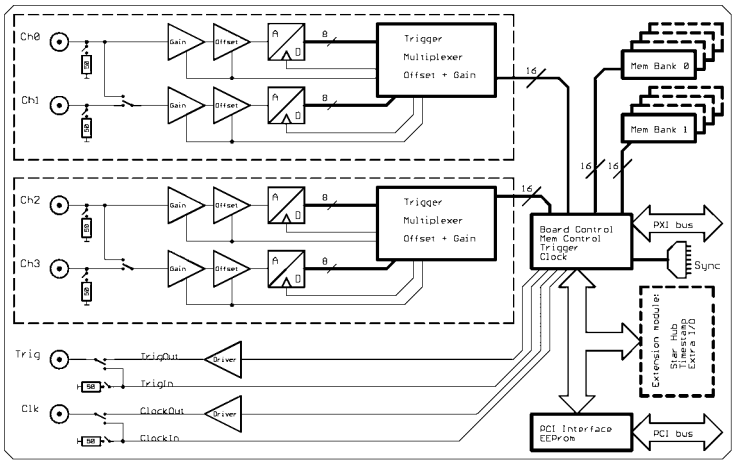
General Information

The 4 models of the UC.2000 series are designed for the fast and high quality data acquisition.

Each channel has its own A/D converter so there is no phase error between channels. The voltage range, signal offset and input impedance can be programmed for each channel to match a wide variety of signal sources.

Data is written in the internal 16 MSamples up to 512 MSample large memory. This memory can also be used as a FIFO buffer so that data can be transferred on-line directly into the PC RAM or to hard disk.

Hardware block diagram



Software programmable parameters

Sampling rate	1 kS/s to max sampling rate, external clock, ref clock
Input Range	±50 mV, ±100 mV, ±200 mV, ±500 mV, ±1 V, ±2 V, ±5 V
Input impedance	50 Ohm / 1 MOhm
Input Offset	±400% in steps of 1%
Clock mode	internal PLL, int.quartz, external, ext. divided, ext. reference clock
Clock impedance	50 Ohm / 1 MOhm
Trigger impedance	50 Ohm / 1 MOhm
Trigger mode	Channel, External, Software, Auto, Windows, Pulse
Trigger level	1/64 to 63/64 of input range (6 bit)
Trigger edge	rising edge, falling edge or both edges
Trigger pulsewidth	1 to 255 samples in steps of 1 sample
Memory depth	64 up to installed memory in steps of 64
Posttrigger	64 up to 128 M in steps of 64
Multiple Recording segmentsize	64 up to installed memory / 2 in steps of 64

Application examples

LDA/PDA	Production test	Laboratory equipment
Radar	Spectroscopy	Test of mobile communication
Ultrasound	Medical equipment	

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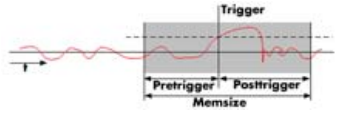
Possibilities and options

Input impedance

All inputs can be individually be switched by software between 50 Ohm and 1 MOhm input impedance. If using fast signals and high sampling rates or you have 50 Ohm cable impedance, then the use of the 50 Ohm termination is recommended to minimise noise and signal reflections. If using weak signal sources or standard probes the use of the 1 MOhm termination is helpful.

Ring buffer mode



The ring buffer mode is the standard mode for all oscilloscope boards. Data is written in a ring memory of the board until a trigger event is detected. After the event the posttrigger values are recorded. This alows the user to record events both before and after the trigger: Pretrigger = Memsize - Posttrigger.

FIFO mode

The FIFO mode is designed for continuous data transfer between measurement board and PC memory (up to 100 MB /s) or hard disk (up to 50 MB/s). The control of the data stream is done automatically by the driver on interrupt request.

Channel trigger

The data acquisition boards offer a wide variety of trigger modes. Besides the standard level and edge triggers known from oscilloscopes, it's also possible to define a window trigger. All trigger modes can be combined with the pulsewidth trigger. This makes it possible to trigger on signal errors like too long or too short pulses.

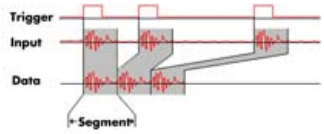
External trigger I/O

All boards can be triggered using an external TTL signal. It's possible to use positive or negative edge also in combination with a programmable pulse width. A softwate trigger event can, when activated by software, be routed to the trigger connector to start external instruments.

Pulse width

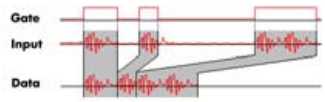
Defines the minimum or maximum width that a trigger pulse must have to generate a trigger event. Pulse width can be combined with channel trigger, pattern trigger and external trigger.

Multiple Recording



The Multiple Recording option allows the recording of several trigger events without restarting the hardware. This enables very fast repetition rates to be achieved. The onboard memory is divided in several segments of same size. Each of them is filled with data if a trigger event occurs.

Gated Sampling

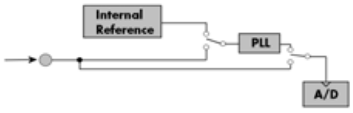


The Gated Sampling option allows data recording controlled by an external gate signal. Data is only recorded if the gate signal has a programmed level.

External clock I/O

Using a dedicated connector a sampling clock can be fed in from an external system. It's also possible to output the internal sampling clock to synchronise external equipment to this clock.

Reference clock



The option to use a precise external reference clock (normally 10 MHz) is necessary to synchronise the board for high-quality measurements with external equipment (like a signal source). It's also possible to enhance the quality of the sampling clock in this way. The driver automatically generates the requested sampling clock from the fed in reference clock.

Cascading

The Cascading option synchronises up to 4 Strategic Test boards internally. It's the easiest way to build up a multi channel system. There is a phase delay between two boards of about 500 pico seconds when this synchronisation option is used.

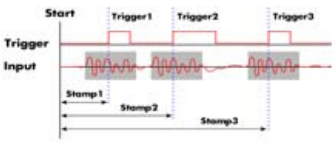
Star Hub

The Star Hub is an additional module allowing the phase stable synchronisation of up to 16 boards. Independent of the number of boards there is no phase delay between all channels. The Star Hub distributes trigger and clock information between all boards. As a result all connected boards are running with the same clock and the same trigger.

Extra I/O

The Extra I/O module adds 24 additional digital I/O lines and 4 analog outputs on an extra connector. These additional lines are independent from the standard function and can be controlled asynchronously. There is also an internal version available with 16 digital I/Os and 4 analog outputs that can be used directly at the rear board connector.

Timestamp



The timestamp option writes the time positions of the trigger events in an extra memory. The timestamps are relative to the start of recording, a defined zero time, externally synchronised to a radio clock, or a GPS receiver. With this option acquisitions of systems on different locations can be set in a precise time relation.

Technical Data

Resolution	8 bit	Dimension	160 mm x 233 mm (Standard 6U)
Differential linearity error (ADC)	0.5 LSB typ.	Width (Standard)	1 slot
Integral linearity error (ADC)	0.5 LSB typ.	Width (with star hub option)	2 slots
Multi: Trigger to 1st sample delay	fixed	Analogue Connector	3 mm SMB male
Multi: Recovery (re-arm) time	< 20 samples	Overvoltage protection (range < ±500 mV)	±5 V
Trigger accuracy 2/4 channel mode	1 Sample	Overvoltage protection (range > ±500 mV)	±50 V
Trigger accuracy 1 channel mode	2 Samples	Warm up time	10 minutes
Ext. clock: delay to internal clock	42 ns ± 2 ns	Operating temperature	0°C - 50°C
input signal with 50 ? termination	max 5 V rms	Storage temperature	-10°C - 70°C
Trigger output delay	1 Sample	Humidity	10% to 90%
Input impedance	50 Ohm / 1 MOhm || 25 pF		
Min internal clock	1 kS/s	Power consumption 3.3 V @ full speed	max. 1.67 A (5.5 Watt)
Min external clock	1 MS/s	Power consumption 5 V @ full speed	max. 1.35 A (6.8 Watt)
Trigger input:Standard TTL level	Low: -0.5 > level < 0.8 V High: 2.0 V > level < 5.5 V Trigger pulse must be valid ≥ 2 clock periods.	Clock input: Standard TTL level	Low: -0.5 V > level < 0.8 V High: 2.0 V > level < 5.5 V Rising edge. Duty cycle: 50% ± 5%
Trigger output	Standard TTL, capable of driving 50 Ohm. Low < 0.4 V (@ 20 mA, max 64 mA) High > 2.4 V (@ -20 mA, max -48 mA) One positive edge after the first internal trigger	Clock output	Standard TTL, capable of driving 50 Ohm Low < 0.4 V (@ 20 mA, max 64 mA) High > 2.4 V (@ -20 mA, max -48 mA)

Input range	±50 mV	±100 mV	±200 mV	±500 mV	±1 V	±2 V	±5 V
Software programmable offset	±200 mV	±400 mV	±800 mV	±2 V	±4 V	±8 V	±20 V
Offset error	< 1 LSB, adjustable by user						
Gain error	< 2 %	< 2 %	< 2 %	< 2 %	< 2 %	< 2 %	< 2 %
UC.202x: Noise (rms): 50 Ohm, 50 MS/s	< 1.0 LSB	< 1.0 LSB	< 1.0 LSB	< 1.0 LSB	< 1.0 LSB	< 1.0 LSB	< 1.0 LSB
UC.203x: Noise (rms): 50 Ohm, 100/200 MS/s	< 2.0 LSB	< 1.5 LSB	< 1.5 LSB	< 1.5 LSB	< 1.5 LSB	< 1.5 LSB	< 1.5 LSB
Crosstalk 5 MHz signal, ±50 mV input, 50 Ohm	< 62 dB						

	UC.2020 UC.2021	UC.2030 UC.2031
max internal clock	50 MS/s	200 MS/s
max external clock	50 MS/s	100 MS/s
-3 dB bandwidth	> 25 MHz	> 90 MHz

Dynamic Parameters

	UC.2020 UC.2021	UC.2030 UC.2031
Test - Sample rate	50 MS/s	100 MS/s
Test signal frequency	1 MHz	1 MHz
SNR (typ)	> 47.5 dB	> 45.9 dB
THD (typ)	< -52.5 dB	< -49.1 dB
SFDR (typ), incl harm.	> 57.0 dB	> 55.5 dB
SINAD (typ)	> 46.0 dB	> 44.2
ENOB (based on SINAD)	> 7.3	> 7.1

Dynamic parameters are measured at ± 1 V input range (if no other range is stated) and 50 Ohm termination with the samplerate specified in the table. Measured parameters are averaged 20 times to get typical values. Test signal is a pure sine wave of the specified frequency with > 99% amplitude. SNR and RMS noise parameters may differ depending on the quality of the used PC. SNR = Signal to Noise Ratio, THD = Total Harmonic Distortion, SFDR = Spurious Free Dynamic Range, SINAD = Signal Noise and Distortion, ENOB = Effective Number of Bits. For a detailed description please see application note 002.

Order information

Order No	Description	Order No	Description
UC2020	UC.2020 with 16 MSample memory and drivers/SBench 5.x	UC2000-32M	Option: 32 MSample mem instead of 16 MSample standard mem
UC2021	UC.2021 with 16 MSample memory and drivers/SBench 5.x	UC2000-64M	Option: 64 MSample mem instead of 16 MSample standard mem
UC2030	UC.2030 with 16 MSample memory and drivers/SBench 5.x	UC2000-128M	Option: 128 MSample mem instead of 16 MSample standard mem
UC2031	UC.2031 with 16 MSample memory and drivers/SBench 5.x	UC2000-256M	Option: 256 MSample mem instead of 16 MSample standard mem
		UC2000-512M	Option: 512 MSample mem instead of 16 MSample standard mem
UC2000-smod	Star Hub: Synchronisation of 2 - 16 boards, one option per system	UC2000-up	Additional handling costs for later memory upgrade
UC2000-xmf	Extra I/O, external connector: 24 DI/O, 4 Analog out, incl. cable		
UC2000-time	Timestamp option: Extra memory for trigger time	UC2000-mr	Option Multiple Recording: Memory segmentation
		UC2000-gs	Option Gated Sampling: Gate signal controls acquisition
Cab-3f-9m-80	Adapter cable: SMB female to BNC male 80 cm	UC2000-cs	Synchronisation of 2 - 4 boards, one option per system
Cab-3f-9m-200	Adapter cable: SMB female to BNC male 200 cm		
Cab-3f-9f-80	Adapter cable: SMB female to BNC female 80 cm	UC2000-dl	DASYLab driver for UC.2000 series
Cab-3f-9f-200	Adapter cable: SMB female to BNC female 200 cm	UC2000-hp	VEE driver for UC.2000 series
		UC2000-lv	LabVIEW driver for UC.2000 series
		UF/UC/UX-ml	MATLAB driver for all UF/UC/UX series.

technical changes and printing errors possible

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