UltraFast

UC.3000 : 12 bit A/D Digitizers, up to 200 MS/s

- **CompactPCI / PXI 6U format**
- **Fastest 12 bit A/D converter board**
- **Up to 200 MS/s on 1 channel**
- **Up to 100 MS/s on 2 channels**
- **Up to 60 MS/s on four channels**
- **Simultaneous sampling on all channels**
- **6 input ranges: ±200 mV up to ± 10 V**
- **Up to 256 MSample memory**
- **FIFO mode for slower sampling rates**
- **Window and pulsewidth trigger**
- **Input offset up to ±100%**
- **Multiple card synchronization option**

Product range overview

The UltraFast CompactPCI cards are based on more than 16 years design experience. The cards are high-quality, low-noise PC-based instruments that have deeper memory and more flexibility than traditional oscilloscopes.

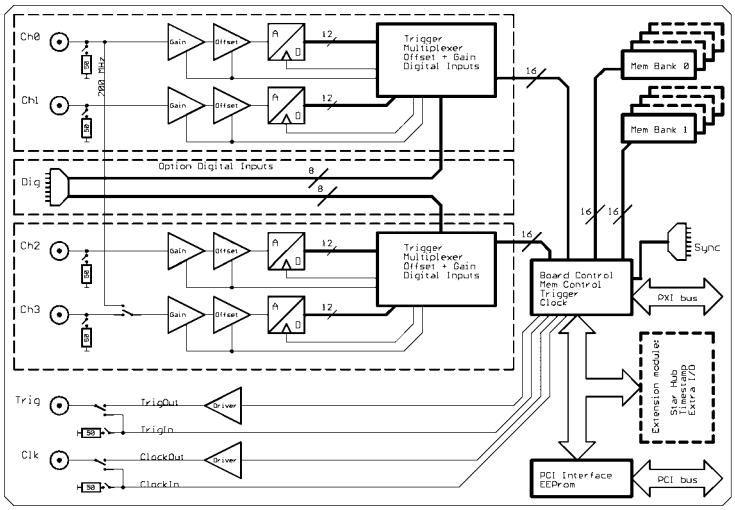
Model	1 channel	2 channels	4 channels
UC.3010	80 MS/s		
UC.3011	40 MS/s	40 MS/s	
UC.3012	80 MS/s	40 MS/s	
UC.3013	40 MS/s	40 MS/s	40 MS/s
UC.3014	80 MS/s	80 MS/s	40 MS/s
UC.3015	160 MS/s	80 MS/s	
UC.3016	160 MS/s	80 MS/s	40 MS/s
UC.3020	100 MS/s		
UC.3021	50 MS/s	50 MS/s	
UC.3022	100 MS/s	50 MS/s	
UC.3023	50 MS/s	50 MS/s	50 MS/s
UC.3024	100 MS/s	100 MS/s	50 MS/s
UC.3025	200 MS/s	100 MS/s	
UC.3026	200 MS/s	100 MS/s	50 MS/s
UC.3027	100 MS/s	100 MS/s	
UC.3031	60 MS/s	60 MS/s	
UC.3033	60 MS/s	60 MS/s	60 MS/s

Software/Drivers

A large number of drivers and examples are delivered with the board or are available as an option:

- Windows 98/ME/NT/2000/XP - drivers
- Linux - drivers
- SBench 5.2
- Streaming Software SPviewIT 6.2 (as option)
- Visual C++/Borland C++ Builder examples
- Borland Delphi examples
- Microsoft Visual Basic examples
- Microsoft Excel examples
- LabWindows/CVI examples
- FlexPro support with SBench
- LabVIEW - drivers (as option)
- DASYLab - drivers (as option)
- MATLAB - drivers (as option)
- Agilent VEE - drivers (as option)

Hardware block diagram



Software programmable parameters

Sampling rate	1 kS/s to max sampling rate, external clock, ref clock
Input Range	±200 mV, ±500 mV, ±1 V, ±2 V, ±5 V, ±10 V
Input impedance	50 Ohm / 1 MOhm
Input Offset	±100% in steps of 1%
Clock mode	internal PLL, int.quartz, external, ext. divided, ext. reference clock
Clock impedance	50 Ohm / 1 MOhm
Trigger impedance	50 Ohm / 1 MOhm
Trigger mode	Channel, External, Software, Auto, Windows, Pulse
Trigger level	1/256 to 255/256 of input range
Trigger edge	rising edge, falling edge or both edges
Trigger pulsewidth	1 to 255 samples in steps of 1 sample
Memory depth	32 up to installed memory in steps of 32
Posttrigger	32 up to 128 M in steps of 32
Multiple Recording segmentsize	32 up to installed memory / 2 in steps of 32

Application examples

LDA/PDA	Production test	Laboratory equipment
Radar	Spectroscopie	Test of mobile communication
Ultrasound	Medical equipment	

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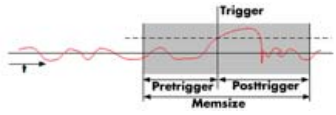
Possibilities and options

Ring buffer mode



The ring buffer mode is the standard mode for all oscilloscope boards. Data is written in a ring memory of the board until a trigger event is detected. After the event the posttrigger values are recorded. This alows the user to record events both before and after the trigger: Pretrigger = Memsize - Posttrigger.

FIFO mode

The FIFO mode is designed for continuous data transfer between measurement board and PC memory (up to 100 MB /s) or hard disk (up to 50 MB/s). The control of the data stream is done automatically by the driver on interrupt request.

Channel trigger

The data acquisition boards offer a wide variety of trigger modes. Besides the standard level and edge triggers known from oscilloscopes, it's also possible to define a window trigger. All trigger modes can be combined with the pulsewidth trigger. This makes it possible to trigger on signal errors like too long or too short pulses.

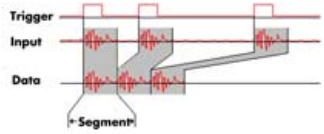
External trigger I/O

All boards can be triggered using an external TTL signal. It's possible to use positive or negative edge also in combination with a programmable pulse width. A softwate trigger event can, when activated by software, be routed to the trigger connector to start external instruments.

Pulse width

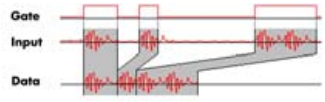
Defines the minimum or maximum width that a trigger pulse must have to generate a trigger event. Pulse width can be combined with channel trigger, pattern trigger and external trigger.

Multiple Recording



The Multiple Recording option allows the recording of several trigger events without restarting the hardware. This enables very fast repetition rates to be achieved. The onboard memory is divided in several segments of same size. Each of them is filled with data if a trigger event occurs.

Gated Sampling

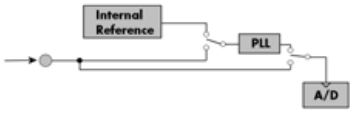


The Gated Sampling option allows data recording controlled by an external gate signal. Data is only recorded if the gate signal has a programmed level.

External clock I/O

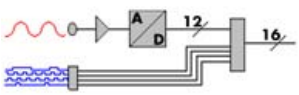
Using a dedicated connector a sampling clock can be fed in from an external system. It's also possible to output the internal sampling clock to synchronise external equipment to this clock.

Reference clock



The option to use a precise external reference clock (normally 10 MHz) is necessary to synchronise the board for high-quality measurements with external equipment (like a signal source). It's also possible to enhance the quality of the sampling clock in this way. The driver automatically generates the requested sampling clock from the fed in reference clock.

Digital inputs



This option adds 4 high-speed digital inputs per channel. These are recorded simultanelously and synchronous with the analog signals.

Cascading

The Cascading option synchronises up to 4 Strategic Test boards internally. It's the easiest way to build up a multi channel system. There is a phase delay between two boards of about 500 pico seconds when this synchronisation option is used.

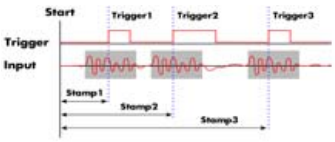
Star Hub

The Star Hub is an additional module allowing the phase stable synchronisation of up to 16 boards. Independent of the number of boards there is no phase delay between all channels. The Star Hub distributes trigger and clock information between all boards. As a result all connected boards are running with the same clock and the same trigger.

Extra I/O

The Extra I/O module adds 24 additional digital I/O lines and 4 analog outputs on an extra connector. These additional lines are independent from the standard function and can be controlled asynchronously. There is also an internal version available with 16 digital I/Os and 4 analog outputs that can be used directly at the rear board connector.

Timestamp



The timestamp option writes the time positions of the trigger events in an extra memory. The timestamps are relative to the start of recording, a defined zero time, externally synchronised to a radio clock, or a GPS receiver. With this option acquisitions of systems on different locations can be set in a precise time relation.

Technical Data

Resolution	12 bit	Input signal with 50 Ohm termination	max 5 V rms
Differential linearity error	≤ 1 LSB (ADC)	Input impedance	50 Ohm / 1 MOhm || 25 pF
Integral linearity error	≤ 1 LSB (ADC)	Overvoltage protection (range ≤ ±1 V)	±5 V
Offset error	adjustable by user	Overvoltage protection (range > ±1 V)	±50 V
Gain error	< 1%	Digital Inputs input impedance	110 Ohm @ 2.5 V
Crosstalk 1 MHz signal, 50 Ohm term	< -70 dB	Digital Inputs delay to analog sample	-12 samples
Multi: Trigger to 1st sample delay	-10 to +20 samples (fix)	Dimension	160 mm x 233 mm (6U standard)
Multi: Recovery time	< 20 samples	Width (Standard)	1 slot
ext. Trigger accuracy (<125 MS/s)	1 Samples	Width (with digital inputs or star hub)	2 slots
ext. Trigger accuracy (>160 MS/s)	2 Samples	Connector	3 mm SMB male
int. Trigger accuracy	1 Sample	Warm up time	10 minutes
Trigger output delay		Operating temperature	0°C - 50°C
Ext. clock: delay to internal clock	42 ns ± 2 ns	Storage temperature	-10°C - 70°C
Min internal clock	1 kS/s	Humidity	10% to 90%
Min external clock	1 MS/s	Power consumption 3.3 V @ full speed	max. 1.53 A (5.1 Watt)
		Power consumption 5 V @ full speed	max. 1.75 A (8.8 Watt)

Trigger input:Standard TTL level	Low: -0.5 > level < 0.8 V High: 2.0 V > level < 5.5 V Trigger pulse must be valid ≥ 2 clock periods.	Clock input: Standard TTL level	Low: -0.5 V > level < 0.8 V High: 2.0 V > level < 5.5 V Rising edge. Duty cycle: 50% ± 5%
Trigger output	Standard TTL, capable of driving 50 Ohm. Low < 0.4 V (@ 20 mA, max 64 mA) High > 2.4 V (@ -20 mA, max -48 mA) One positive edge after the first internal trigger	Clock output	Standard TTL, capable of driving 50 Ohm Low < 0.4 V (@ 20 mA, max 64 mA) High > 2.4 V (@ -20 mA, max -48 mA)

	UC.3011 UC.3013	UC.3021 UC.3023	UC.3031 UC.3033	UC.3010 UC.3012 UC.3014	UC.3020 UC.3022 UC.3024 UC.3027	UC.3015 UC.3016	UC.3025 UC.3026
max internal clock	40 MS/s	50 MS/s	62.5 MS/s	80 MS/s	100 MS/s	160 MS/s	200 MS/s
max external clock	40 MS/s	50 MS/s	62.5 MS/s	80 MS/s	100 MS/s	80 MS/s	100 MS/s
-3 dB bandwidth	> 20 MHz	> 25 MHz	> 30 MHz	> 40 MHz	> 40 MHz	> 40 MHz	> 40 MHz
Zero noise level (< 125 MS/s)	< 1.5 LSB rms	< 1.5 LSB rms	< 1.75 LSB rms	< 2.0 LSB rms	< 2.0 LSB rms	< 2.0 LSB rms	< 2.0 LSB rms
Zero noise level (> 125 MS/s)	n.a.	n.a.	n.a.	n.a.	n.a.	< 3.0 LSB rms	< 3.0 LSB rms

Dynamic Parameters

	UC.3011 UC.3013	UC.3021 UC.3023	UC.3031 UC.3033	UC.3010 UC.3012 UC.3014	UC.3020 UC.3022 UC.3024 UC.3027	UC.3015 UC.3016	UC.3025 UC.3026
Test - Sample rate	40 MS/s	50 MS/s	60 MS/s	80 MS/s	100 MS/s	80 MS/s	100 MS/s
Test signal frequency	1 MHz	1 MHz	1 MHz	1 MHz	1 MHz	1 MHz	1 MHz
SNR (typ)	> 64.8 dB	> 64.8 dB	> 63.3 dB	> 64.8 dB	> 64.7 dB	> 64.8 dB	> 63.9 dB
THD (typ)	< -73.8 dB	< -73.8 dB	< -73.2 dB	< -73.8 dB	< -73.8 dB	< -73.9 dB	< -73.5 dB
SFDR (typ), excl harm.	> 77.5 dB	> 77.5 dB	> 74.3 dB	> 77.1 dB	> 76.8 dB	> 77.0 dB	> 74.3 dB
SINAD (typ)	> 64.3 dB	> 64.3 dB	> 62.9 dB	> 64.3 dB	> 64.2 dB	> 64.3 dB	> 63.4 dB
ENOB (based on SINAD)	> 10.4 LSB	> 10.4 LSB	> 10.2 LSB	> 10.4 LSB	> 10.4 LSB	> 10.4 LSB	> 10.2 LSB

Dynamic parameters are measured at ± 1 V input range (if no other range is stated) and 50 Ohm termination with the samplerate specified in the table. Measured parameters are averaged 20 times to get typical values. Test signal is a pure sine wave of the specified frequency with > 99% amplitude. SNR and RMS noise parameters may differ depending on the quality of the used PC. SNR = Signal to Noise Ratio, THD = Total Harmonic Distortion, SFDR = Spurious Free Dynamic Range, SINAD = Signal Noise and Distortion, ENOB = Effective Number of Bits. For a detailed description please see application note 002.

Order information

Order No	Description	Order No	Description
UC3010	UC.3010 with 8 MSample memory and drivers/SBench 5.x	UC3000-16M	Option: 16 MSample memory instead of 8 MSample standard mem
UC3011	UC.3011 with 8 MSample memory and drivers/SBench 5.x	UC3000-32M	Option: 32 MSample memory instead of 8 MSample standard mem
UC3012	UC.3012 with 8 MSample memory and drivers/SBench 5.x	UC3000-64M	Option: 64 MSample memory instead of 8 MSample standard mem
UC3013	UC.3013 with 8 MSample memory and drivers/SBench 5.x	UC3000-128M	Option: 128 MSample memory instead of 8 MSample standard mem
UC3014	UC.3014 with 8 MSample memory and drivers/SBench 5.x	UC3000-256M	Option: 256 MSample memory instead of 8 MSample standard mem
UC3015	UC.3015 with 8 MSample memory and drivers/SBench 5.x	UC3000-up	Additional handling costs for later memory upgrade
UC3016	UC.3016 with 8 MSample memory and drivers/SBench 5.x		
UC3020	UC.3020 with 8 MSample memory and drivers/SBench 5.x	UC3000-mr	Option Multiple Recording: Memory segmentation
UC3021	UC.3021 with 8 MSample memory and drivers/SBench 5.x	UC3000-gs	Option Gated Sampling: Gate signal controls acquisition
UC3022	UC.3022 with 8 MSample memory and drivers/SBench 5.x	UC3000-dig	Additional 4 synchronous digital inputs per channel, incl. cable
UC3023	UC.3023 with 8 MSample memory and drivers/SBench 5.x	UC3000-cs	Synchronisation of 2 - 4 boards, one option per system
UC3024	UC.3024 with 8 MSample memory and drivers/SBench 5.x	UC.3000-hbw	100 MHz bandwidth for UC.3025/26 at fixed ±500 mV input
UC3025	UC.3025 with 8 MSample memory and drivers/SBench 5.x	UC3000-dl	DASYLab driver for UC.3000 series
UC3026	UC.3026 with 8 MSample memory and drivers/SBench 5.x	UC3000-hp	VEE driver for UC.3000 series
UC3027	UC.3027 with 8 MSample memory and drivers/SBench 5.x	UC3000-lv	LabVIEW driver for UC.3000 series
UC3031	UC.3031 with 8 MSample memory and drivers/SBench 5.x	UF/UC/UCX-ml	MATLAB driver for all UF/UC/UX series.
UC3033	UC.3033 with 8 MSample memory and drivers/SBench 5.x	UC3000-time	Timestamp option: Extra memory for trigger time
UC3000-smod	Star Hub: Synchronisation of 2 - 16 boards, one option per system	Cab-3f-9m-200	Adapter cable: SMB female to BNC male 200 cm
UC3000-xmf	Extra I/O, external connector: 24 DI/O, 4 Analog out, incl. cable	Cab-3f-9f-80	Adapter cable: SMB female to BNC female 80 cm
Cab-3f-9m-80	Adapter cable: SMB female to BNC male 80 cm	Cab-3f-9f-200	Adapter cable: SMB female to BNC female 200 cm

technical changes and printing errors possible

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