UC.4000 : 14 bit A/D Digitizers, up to 50 MS/s

- **CompactPCI 6U format**
- **Fastest 14 bit A/D converter board**
- **Models with 20 MS/s or 50 MS/s**
- **1, 2 or 4 channels acquisition**
- **Simultaneous sampling on all channels**
- **6 input ranges: ±200 mV up to ± 10 V**
- **Up to 256 MSample memory**
- **FIFO mode**
- **Window and pulsewidth trigger**
- **Input offset up to ±200%**
- **Multiple card synchronization option**
- **Windows program SBench 5.x included**

Product range overview

Model	1 channel	2 channels	4 channels
UC.4020	20 MS/s		
UC.4021	20 MS/s	20 MS/s	
UC.4022	20 MS/s	20 MS/s	20 MS/s
UC.4030	50 MS/s		
UC.4031	50 MS/s	50 MS/s	
UC.4032	50 MS/s	50 MS/s	50 MS/s

Software/Drivers

A large number of drivers and examples are delivered with the board or are available as an option:

- Windows 98/ME/NT/2000/XP - drivers
- Linux - drivers
- SBench 5.2
- Streaming Software SPviewIT 6.2 (as option)
- Visual C++/Borland C++ Builder examples
- Borland Delphi examples
- Microsoft Visual Basic examples
- Microsoft Excel examples
- LabWindows/CVI examples
- FlexPro support with SBench
- LabVIEW - drivers (as option)
- DASYLab - drivers (as option)
- MATLAB - drivers (as option)
- Agilent VEE - drivers (as option)

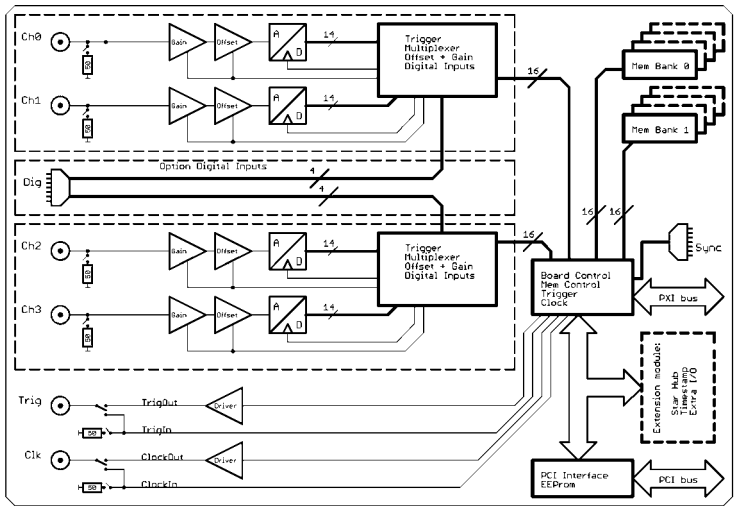
General Information

The UC.4000 boards are most suitable for applications that need high sampling rates as well as a maximum signal dynamic. These boards offer a resolution 4 times higher than 12 bit boards.

Each channel has its own A/D converter so there is no phase error between channels. The voltage range, signal offset and input impedance can be programmed for each channel to match a wide variety of signal sources.

Data is written in the internal 8 MSamples up to 256 MSample card memory. This memory can also be used as a FIFO buffer so that data can be transferred on-line directly into the PC RAM or to hard disk.

Hardware block diagram



Software programmable parameters

Sampling rate	1 kS/s to max sampling rate, external clock, ref clock
Input Range	±200 mV, ±500 mV, ±1 V, ±2 V, ±5 V, ±10 V
Input impedance	50 Ohm / 1 MOhm
Input Offset	±200% in steps of 1%
Clock mode	internal PLL, int.quartz, external, ext. divided, ext. reference clock
Clock impedance	50 Ohm / 1 MOhm
Trigger impedance	50 Ohm / 1 MOhm
Trigger mode	Channel, External, Software, Auto, Windows, Pulse
Trigger level	1/1024 to 1023/1024 of input range (10 bit)
Trigger edge	rising edge, falling edge or both edges
Trigger pulsewidth	1 to 255 samples in steps of 1 sample
Memory depth	32 up to installed memory in steps of 32
Posttrigger	32 up to 128 M in steps of 32
Multiple Recording segmentsize	32 up to installed memory / 2 in steps of 32

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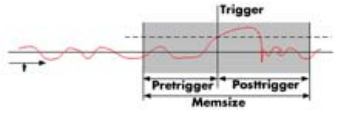
Possibilities and options

Input impedance

All inputs can be individually be switched by software between 50 Ohm and 1 MOhm input impedance. If using fast signals and high sampling rates or you have 50 Ohm cable impedance, then the use of the 50 Ohm termination is recommended to minimise noise and signal reflections. If using weak signal sources or standard probes the use of the 1 MOhm termination is helpful.

Ring buffer mode



The ring buffer mode is the standard mode for all oscilloscope boards. Data is written in a ring memory of the board until a trigger event is detected. After the event the posttrigger values are recorded. This alows the user to record events both before and after the trigger: Pretrigger = Memsize - Posttrigger.

FIFO mode

The FIFO mode is designed for continuous data transfer between measurement board and PC memory (up to 100 MB /s) or hard disk (up to 50 MB/s). The control of the data stream is done automatically by the driver on interrupt request.

Channel trigger

The data acquisition boards offer a wide variety of trigger modes. Besides the standard level and edge triggers known from oscilloscopes, it's also possible to define a window trigger. All trigger modes can be combined with the pulsewidth trigger. This makes it possible to trigger on signal errors like too long or too short pulses.

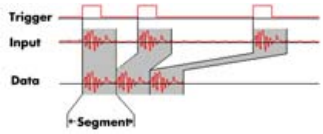
External trigger I/O

All boards can be triggered using an external TTL signal. It's possible to use positive or negative edge also in combination with a programmable pulse width. A softwate trigger event can, when activated by software, be routed to the trigger connector to start external instruments.

Pulse width

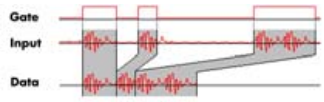
Defines the minimum or maximum width that a trigger pulse must have to generate a trigger event. Pulse width can be combined with channel trigger, pattern trigger and external trigger.

Multiple Recording



The Multiple Recording option allows the recording of several trigger events without restarting the hardware. This enables very fast repetition rates to be achieved. The onboard memory is divided in several segments of same size. Each of them is filled with data if a trigger event occurs.

Gated Sampling

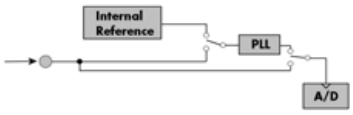


The Gated Sampling option allows data recording controlled by an external gate signal. Data is only recorded if the gate signal has a programmed level.

External clock I/O

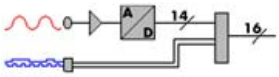
Using a dedicated connector a sampling clock can be fed in from an external system. It's also possible to output the internal sampling clock to synchronise external equipment to this clock.

Reference clock



The option to use a precise external reference clock (normally 10 MHz) is necessary to synchronise the board for high-quality measurements with external equipment (like a signal source). It's also possible to enhance the quality of the sampling clock in this way. The driver automatically generates the requested sampling clock from the fed in reference clock.

Digital inputs



This option provides additional synchronous digital channels phase-stable with the analog data. When the option is installed there are 2 additional digital inputs for every analog A/D channel.

Cascading

The Cascading option synchronises up to 4 Strategic Test boards internally. It's the easiest way to build up a multi channel system. There is a phase delay between two boards of about 500 pico seconds when this synchronisation option is used.

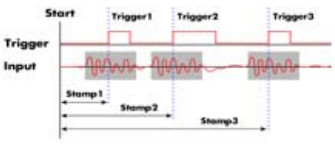
Star Hub

The Star Hub is an additional module allowing the phase stable synchronisation of up to 16 boards. Independent of the number of boards there is no phase delay between all channels. The Star Hub distributes trigger and clock information between all boards. As a result all connected boards are running with the same clock and the same trigger.

Extra I/O

The Extra I/O module adds 24 additional digital I/O lines and 4 analog outputs on an extra connector. These additional lines are independent from the standard function and can be controlled asynchronously. There is also an internal version available with 16 digital I/Os and 4 analog outputs that can be used directly at the rear board connector.

Timestamp



The timestamp option writes the time positions of the trigger events in an extra memory. The timestamps are relative to the start of recording, a defined zero time, externally synchronised to a radio clock, or a GPS receiver. With this option acquisitions of systems on different locations can be set in a precise time relation.

Technical Data

Resolution	14 bit	Dimension	160 mm x 233 mm (Standrad 6U)
Differential linearity error	± 0.5 LSB typ. (ADC)	Width (Standard)	1 slot
Integral linearity error	± 1 LSB typ (ADC)	Width (with digital inputs)	2 slots
Multi: Trigger to 1st sample delay	fixed	Width (with star hub option)	2 slots
Multi: Recovery time	< 20 samples	Analogue Connector	3 mm SMB male
ext. Trigger accuracy	1 Sample	Digital Connector	40 pol half pitch (Hirose FX2 series)
int. Trigger accuracy	1 Sample	Digital Inputs delay to analog sample	-6 samples
Ext. clock: delay to internal clock	42 ns ± 2 ns	Overvoltage protection (range ≤ ±1 V)	±5 V
input signal with 50 W termination	max 5 V rms	Overvoltage protection (range > ±1 V)	±50 V
Trigger output delay	1 Sample	Warm up time	10 minutes
Input impedance	50 Ohm / 1 MOhm || 25 pF	Operating temperature	0°C - 50°C
Crosstalk 1 MHz sine signal 50 Ohm	< -80 dB	Storage temperature	-10°C - 70°C
Crosstalk 1 MHz sine signal 1 MOhm	< -65 dB	Humidity	10% to 90%
Min internal clock	1 kS/s	Zero offset error	adjustable by user
Min external clock	500 kS/s	Gain error	< 1 % of full scale
		Power consumption 3.3 V @ full speed	max. 1.57 A (5.2 Watt)
		Power consumption 5 V @ full speed	max. 1.91 A (9.6 Watt)
Trigger input:Standard TTL level	Low: -0.5 > level < 0.8 V High: 2.0 V > level < 5.5 V Trigger pulse must be valid ≥ 2 clock periods.	Clock input: Standard TTL level	Low: -0.5 V > level < 0.8 V High: 2.0 V > level < 5.5 V Rising edge. Duty cycle: 50% ± 5%
Trigger output	Standard TTL, capable of driving 50 Ohm. Low < 0.4 V (@ 20 mA, max 64 mA) High > 2.4 V (@ -20 mA, max -48 mA) One positive edge after the first internal trigger	Clock output	Standard TTL, capable of driving 50 Ohm Low < 0.4 V (@ 20 mA, max 64 mA) High > 2.4 V (@ -20 mA, max -48 mA)

	UC.4020 UC.4021	UC.4022	UC.4030 UC.4031	UC.4032
max internal clock	20 MS/s	20 MS/s	50 MS/s	50 MS/s
max external clock	20 MS/s	20 MS/s	50 MS/s	50 MS/s
-3 dB bandwidth	> 10 MHz	> 10 MHz	> 25 MHz	> 25 MHz
Zero noise level at 50 Ohm	< 2.1 LSB rms	< 2.6 LSB rms	< 2.9 LSB rms	< 3.6 LSB rms

Dynamic Parameters

	UC.4020 UC.4021	UC.4022	UC.4030 UC.4031	UC.4032
Test - Sample rate	20 MS/s	20 MS/s	50 MS/s	50 MS/s
Test signal frequency	1 MHz	1 MHz	1 MHz	1 MHz
SNR (typ)	> 70.3 dB	> 70.1 dB	> 67.1 dB	> 65.5 dB
THD (typ)	< -73.0 dB	< -73.0 dB	< -72.8 dB	< - 72.8 dB
SFDR (typ), excl harm.	> 82.8 dB dB	> 82.3 dB	> 75.8 dB	> 75.2 dB
SINAD (typ)	> 68.4 dB	> 68.3 dB	> 66.1 dB	> 64.8 dB
ENOB (based on SINAD)	> 11.1	> 11.1	> 10.7	> 10.5

Dynamic parameters are measured at ± 1 V input range (if no other range is stated) and 50 Ohm termination with the samplerate specified in the table. Measured parameters are averaged 20 times to get typical values. Test signal is a pure sine wave of the specified frequency with > 99% amplitude. SNR and RMS noise parameters may differ depending on the quality of the used PC. SNR = Signal to Noise Ratio, THD = Total Harmonic Distortion, SFDR = Spurious Free Dynamic Range, SINAD = Signal Noise and Distortion, ENOB = Effective Number of Bits. For a detailed description please see application note 002.

Order information

Order No	Description	Order No	Description
UC4020	UC.4020 with 8 MSample memory and drivers/SBench 5.x	UC4000-16M	Option: 16 MSample memory instead of 8 MSample standard mem
UC4021	UC.4021 with 8 MSample memory and drivers/SBench 5.x	UC4000-32M	Option: 32 MSample memory instead of 8 MSample standard mem
UC4022	UC.4022 with 8 MSample memory and drivers/SBench 5.x	UC4000-64M	Option: 64 MSample memory instead of 8 MSample standard mem
UC4030	UC.4030 with 8 MSample memory and drivers/SBench 5.x	UC4000-128M	Option: 128 MSample memory instead of 8 MSample standard mem
UC4031	UC.4031 with 8 MSample memory and drivers/SBench 5.x	UC4000-256M	Option: 256 MSample memory instead of 8 MSample standard mem
UC4032	UC.4032 with 8 MSample memory and drivers/SBench 5.x	UC4000-up	Additional handling costs for later memory upgrade
UC4000-smod	Star Hub: Synchronisation of 2 - 16 boards, one option per system	UC4000-mr	Option Multiple Recording: Memory segmentation
UC4000-time	Timestamp option: Extra memory for trigger time	UC4000-gs	Option Gated Sampling: Gate signal controls acquisition
UC4000-xmf	Extra I/O, external connector: 24 DI/O, 4 Analog out, incl. cable	UC4000-dig	Additional 4 synchronous digital inputs per channel, incl. cable
		UC4000-cs	Synchronisation of 2 - 4 boards, one option per system
Cab-3f-9m-80	Adapter cable: SMB female to BNC male 80 cm	UC4000-dl	DASYLab driver for UC.4000 series
Cab-3f-9m-200	Adapter cable: SMB female to BNC male 200 cm	UC4000-hp	VEE driver for UC.4000 series
Cab-3f-9f-80	Adapter cable: SMB female to BNC female 80 cm	UC4000-lv	LabVIEW driver for UC.4000 series
Cab-3f-9f-200	Adapter cable: SMB female to BNC female 200 cm	UF/UXC/UX-ml	MATLAB driver for all UDF/UC/UX series.

technical changes and printing errors possible

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