UltraFast

UC.4600 : 16 bit A/D Digitizer cards, to 3 MS/s

- **CompactPCI 6U format**
- **2, 4 or 8 channels with 16 bit resolution per card**
- **Versions with 200 kS/s up to 3 MS/s**
- **Simultaneous sampling on all channels**
- **Software selectable single-ended or differential inputs**
- **Separate ADC and amplifier per channel**
- **Complete on-board calibration**
- **8 input ranges: ±50 mV up to ±10 V**
- **Up to 256 MSample (512 MByte) on-board memory**
- **Sustained streaming mode up to 100 MB/s**
- **Window, pulse width, re-arm, spike, OR/AND trigger**
- **Programmable input offset of ±5 V**
- **Multiple card synchronization option**

Product range overview

Model	1 channel	2 channels	4 channels	8 channels
UC.4620	200 kS/s	200 kS/s		
UC.4621	200 kS/s	200 kS/s	200 kS/s	
UC.4622	200 kS/s	200 kS/s	200 kS/s	200 kS/s
UC.4630	500 kS/s	500 kS/s		
UC.4631	500 kS/s	500 kS/s	500 kS/s	
UC.4632	500 kS/s	500 kS/s	500 kS/s	500 kS/s
UC.4640	1 MS/s	1 MS/s		
UC.4641	1 MS/s	1 MS/s	1 MS/s	
UC.4642	1 MS/s	1 MS/s	1 MS/s	1 MS/s
UC.4650	3 MS/s	3 MS/s		
UC.4651	3 MS/s	3 MS/s	3 MS/s	
UC.4652	3 MS/s	3 MS/s	3 MS/s	3 MS/s

Software/Drivers

A large number of drivers and examples are delivered with the board or are available as an option:

- Windows 98/ME/NT/2000/XP - drivers
- Linux - drivers
- SBench 5.2
- Streaming Software SPviewIT 6.2 (as option)
- Visual C++/Borland C++ Builder examples
- Borland Delphi examples
- Microsoft Visual Basic examples
- Microsoft Excel examples
- LabWindows/CVI examples
- FlexPro support with SBench
- LabVIEW - drivers (as option)
- DASYLab - drivers (as option)
- MATLAB - drivers (as option)
- Agilent VEE - drivers (as option)

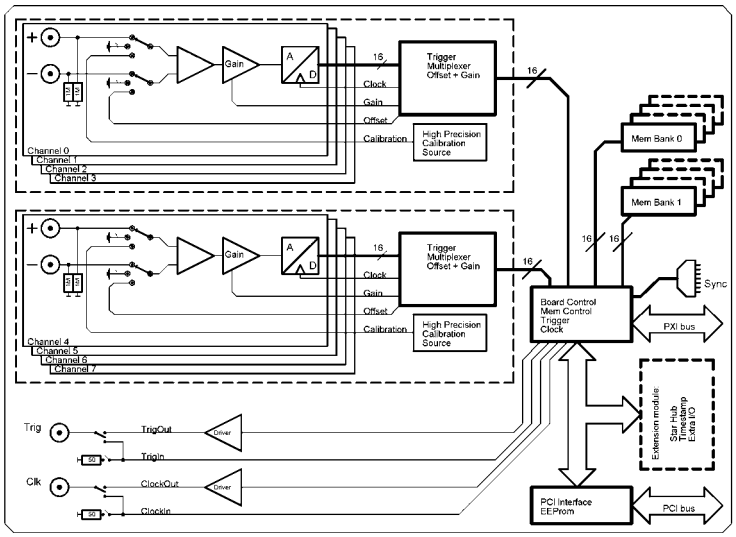
General Information

The UC.4600 for the first time offers 16 bit resolution synchronously on up to 8 channels at up to 3 MS/s.

Each channel has its own A/D converter so there is no phase error between channels. The voltage range, signal offset and input impedance can be programmed for each channel to match a wide variety of signal sources.

Data is written in the internal 8 MSamples up to 256 MSample card memory. This memory can also be used as a FIFO buffer so that data can be transferred on-line directly into the PC RAM or to hard disk.

Hardware block diagram



Software programmable parameters

Sampling rate	1 kS/s to max sampling rate, external clock, ref clock
Input range	±50 mV, ±100 mV, ±250 mV, ±500 mV, ±1 V, ±2 V, ±5 V, ±10 V
Input Offset (single-ended)	programmable to ±5 V in steps of 1 mV, not exceeding ±10 V input
Input type	Single-ended, true differential
Clock mode	internal PLL, internal quartz, external, external divided, external reference clock
Clock impedance	50 Ohm / 1 MOhm
Trigger impedance	50 Ohm / 1 MOhm
Trigger mode	Channel, External, Software, Auto, Window, Pulse, Spike
Trigger level resolution	14 bit
Trigger edge	rising edge, falling edge or both edges
Trigger pulsewidth	1 to 255 samples in steps of 1 sample
Memory depth	32 up to installed memory in steps of 32
Posttrigger	32 up to 128 M in steps of 32
Multiple Recording segmentsize	32 up to installed memory / 2 in steps of 32

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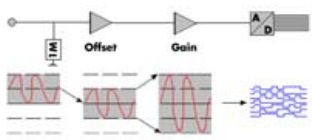
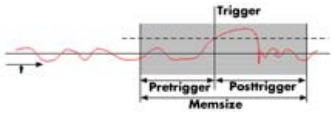
Possibilities and options

Input Amplifier



The analog inputs can be adapted to real world signals using a wide variety of settings that are individual for each channel. By using software commands one can select a matching input range and the signal offset can be compensated.

Ring buffer mode



The ring buffer mode is the standard mode for all oscilloscope boards. Data is written in a ring memory of the board until a trigger event is detected. After the event the posttrigger values are recorded. This alows the user to record events both before and after the trigger: Pretrigger = Memsize - Posttrigger.

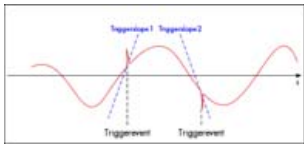
FIFO mode

The FIFO mode is designed for continuous data transfer between measurement board and PC memory (up to 100 MB /s) or hard disk (up to 50 MB/s). The control of the data stream is done automatically by the driver on interrupt request.

Channel trigger

The data acquisition boards offer a wide variety of trigger modes. Besides the standard level and edge triggers known from oscilloscopes, it's also possible to define a window trigger. All trigger modes can be combined with the pulsewidth trigger. This makes it possible to trigger on signal errors like too long or too short pulses.

Spike trigger



When using the spike trigger mode, the difference between two samples is checked whether being higher than the programmed limit or not. This can be useful to trigger e.g. on noise coming from a power supply.

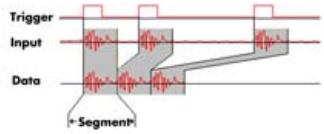
External trigger I/O

All boards can be triggered using an external TTL signal. It's possible to use positive or negative edge also in combination with a programmable pulse width. A softwate trigger event can, when activated by software, be routed to the trigger connector to start external instruments.

Pulse width

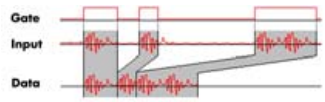
Defines the minimum or maximum width that a trigger pulse must have to generate a trigger event. Pulse width can be combined with channel trigger, pattern trigger and external trigger.

Multiple Recording



The Multiple Recording option allows the recording of several trigger events without restarting the hardware. This enables very fast repetition rates to be achieved. The onboard memory is divided in several segments of same size. Each of them is filled with data if a trigger event occurs.

Gated Sampling

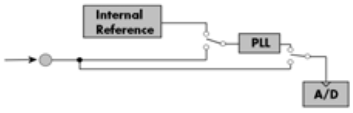


The Gated Sampling option allows data recording controlled by an external gate signal. Data is only recorded if the gate signal has a programmed level.

External clock I/O

Using a dedicated connector a sampling clock can be fed in from an external system. It's also possible to output the internal sampling clock to synchronise external equipment to this clock.

Reference clock



The option to use a precise external reference clock (normally 10 MHz) is necessary to synchronise the board for high-quality measurements with external equipment (like a signal source). It's also possible to enhance the quality of the sampling clock in this way. The driver automatically generates the requested sampling clock from the fed in reference clock.

Cascading

The Cascading option synchronises up to 4 Strategic Test boards internally. It's the easiest way to build up a multi channel system. There is a phase delay between two boards of about 500 pico seconds when this synchronisation option is used.

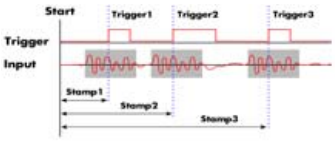
Star Hub

The Star Hub is an additional module allowing the phase stable synchronisation of up to 16 boards. Independent of the number of boards there is no phase delay between all channels. The Star Hub distributes trigger and clock information between all boards. As a result all connected boards are running with the same clock and the same trigger.

Extra I/O

The Extra I/O module adds 24 additional digital I/O lines and 4 analog outputs on an extra connector. These additional lines are independent from the standard function and can be controlled asynchronously. There is also an internal version available with 16 digital I/Os and 4 analog outputs that can be used directly at the rear board connector.

Timestamp



The timestamp option writes the time positions of the trigger events in an extra memory. The timestamps are relative to the start of recording, a defined zero time, externally synchronised to a radio clock, or a GPS receiver. With this option acquisitions of systems on different locations can be set in a precise time relation.

Differential inputs

With a simple software command the inputs can individually be switched from single-ended (in relation to ground) to differential, without losing any inputs. When the inputs are used in differential mode the A/D converter measures the difference between two lines with relation to system ground.

Technical Data

Analog Inputs

Resolution	16 bit
Inputs	True differential / single-ended
Differential non linearity (DNL)	465x: ±2 LSB, all others ±1 LSB (ADC)
Integral non linearity (INL)	465x: ±2 LSB, all others ±1 LSB (ADC)
Offset error (full speed)	≤ 1 LSB (after calibration)
Gain error (full speed)	≤ 0.1% (after calibration)
Programmable input offset	±5 V for single-ended ranges < ±10 V
Crosstalk: all ranges 100 kHz signal	≤ -110 dB on adjacent channels, 50 ohm term.
Analog Input impedance	1 MOhm against GND
Over voltage protection	±30 V all ranges (activated card)
CMRR for ±50 mV to ±500 mV	> 70 dB
CMRR for ±1 V to ±10 V	> 46 dB
Connector (analog)	MMCX female
Connector (trigger/clock)	3 mm SMB male

Power consumption (max speed)	**3,3 V**	**5 V**	**-12 V**	**+12 V**	**Total**
UC.46x0 (8 MS memory)	TDB	TDB	TDB	TDB	TDB
UC.46x1 (8 MS memory)	TDB	TDB	TDB	TDB	TDB
UC.46x2 (8 MS memory)	TDB	TDB	TDB	TDB	TDB
UC.4652 (256 MS memory),max power	TDB	TDB	TDB	TDB	TDB

Trigger input:Standard TTL level	Low: -0.5 > level < 0.8 V High: 2.0 V > level < 5.5 V Trigger pulse must be valid ≥ 2 clock periods.
Trigger output	Standard TTL, capable of driving 50 Ohm. Low < 0.4 V (@ 20 mA, max 64 mA) High > 2.4 V (@ -20 mA, max -48 mA) One positive edge after the first internal trigger

Ext. clock: delay to internal clock	42 ns ± 2 ns

Trigger

Multi: Trigger to 1st sample delay	fixed
Multi: Recovery time	< 20 samples
ext. Trigger accuracy	1 Sample
int. Trigger accuracy	1 Sample
input signal with 50 ohm termination	max 5 V rms
Trigger output delay	1 Sample

Environmental and Physical details

Dimension	160 mm x 233 mm (Standard 6U)
Width (standard board)	1 slot
Width (with star hub)	2 slots
Warm up time	10 minutes
Operating temperature	0°C - 50°C
Storage temperature	-10°C - 70°C
Humidity	10% to 90%

Certifications and Compliances

EMC Immunity	Compliant with CE Mark
EMC Emission	Compliant with CE Mark

Clock input: Standard TTL level	Low: -0.5 V > level < 0.8 V High: 2.0 V > level < 5.5 V Rising edge. Duty cycle: 50% ± 5%
Clock output	Standard TTL, capable of driving 50 Ohm Low < 0.4 V (@ 20 mA, max 64 mA) High > 2.4 V (@ -20 mA, max -48 mA)

	UC.4620 UC.4621 UC.4622	UC.4630 UC.4631 UC.4632	UC.4640 UC.4641 UC.4642	UC.4650 UC.4651 UC.4652
Min internal clock	1 kS/s	1 kS/s	1 kS/s	1 kS/s
Max internal clock	200 kS/s	500 kS/s	1 MS/s	3 MS/s
Min external clock	1 kS/s	1 kS/s	1 kS/s	1 kS/s
Max external clock	200 kS/s	500 kS/s	1 MS/s	3 MS/s
-3 dB bandwidth	> 100 kHz	> 250 kHz	> 500 kHz	> 1.5 MHz

Dynamic Parameters

	UC.4620 UC.4621 UC.4622	UC.4630 UC.4631 UC.4632	UC.4640 UC.4641 UC.4642	UC.4650 UC.4651 UC.4652
Test - sampling rate	200 kS/s	500 kS/s	1 MS/s	3 MS/s
Test signal frequency	TBD	TBD	TBD	TBD
SNR (typ)	TBD	TBD	TBD	TBD
THD (typ)	TBD	TBD	TBD	TBD
SFDR (typ), incl harm.	TBD	TBD	TBD	TBD
SINAD (typ)	TBD	TBD	TBD	TBD
ENOB (based on SINAD)	TBD	TBD	TBD	TBD

Dynamic parameters are measured at ±5 V input range (if no other range is stated) and 1 MOhm termination with the sampling rate specified in the table. Measured parameters are averaged 20 times to get typical values. Test signal is a pure sine wave of the specified frequency with > 99% amplitude. SNR and RMS noise parameters may differ depending on the quality of the used PC. SNR = Signal to Noise Ratio, THD = Total Harmonic Distortion, SFDR = Spurious Free Dynamic Range, SINAD = Signal Noise and Distortion, ENOB = Effective Number of Bits. For a detailed description please see application note 002.

Order Information

Versions

Order no.	1 channel	2 channels	4 channels	8 channels
UC.4620	200 kS/s	200 kS/s		
UC.4621	200 kS/s	200 kS/s	200 kS/s	
UC.4622	200 kS/s	200 kS/s	200 kS/s	200 kS/s
UC.4630	500 kS/s	500 kS/s		
UC.4631	500 kS/s	500 kS/s	500 kS/s	
UC.4632	500 kS/s	500 kS/s	500 kS/s	500 kS/s
UC.4640	1 MS/s	1 MS/s		
UC.4641	1 MS/s	1 MS/s	1 MS/s	
UC.4642	1 MS/s	1 MS/s	1 MS/s	1 MS/s
UC.4650	3 MS/s	3 MS/s		
UC.4651	3 MS/s	3 MS/s	3 MS/s	
UC.4652	3 MS/s	3 MS/s	3 MS/s	3 MS/s

Memory

Order no.	Option
UC.4600-16M	Memory upgrade to 16 MSample (32 MB) of total memory
UC.4600-32M	Memory upgrade to 32 MSample (64 MB) of total memory
UC.4600-64M	Memory upgrade to 64 MSample (128 MB) of total memory
UC.4600-128M	Memory upgrade to 128 MSample (256 MB) of total memory
UC.4600-256M	Memory upgrade to 256 MSample (512 MB) of total memory
UC.4600-up	Additional fee for later memory upgrade

Options

Order no.	Option
UC.4600-mr	Option Multiple Recording
UC.4600-gs	Option Gated Sampling
UC.4600-cs	Option Cascading: Synchronization of up to 4 cards (one option needed per system)
UC.4600-smod (1)	Option Star-Hub:Synchronization of up to 16 cards (one option needed per system)
UC.4600-time (1)	Option Timestamp: Recording of trigger timestamps in an extra memory
UC.4600-xmf (1)	Option Extra I/O with external connector, 24 digital I/O + 4 analog outputs. Including one cable Cab-d40-idc-100.

Cables

Order no.	Option
Cab-1m-9m-80	Adapter cable MMCX male to BNC male, 80 cm (for analog inputs)
Cab-1m-9f-80	Adapter cable MMCX male to BNC female, 80 cm (for analog inputs)
Cab-1m-9m-200	Adapter cable MMCX male to BNC male, 200 cm (for analog inputs)
Cab-1m-9f-200	Adapter cable MMCX male to BNC female, 200 cm (for analog inputs)
Cab-1m-9f-5	Adapter cable MMCX male to BNC female, 5 cm (short cable especially for oscilloscope probes)
Cab-3f-9m-80	Adapter cable SMB female to BNC male, 80 cm (for clock and trigger I/O)
Cab-3f-9f-80	Adapter cable SMB female to BNC female, 80 cm (for clock and trigger I/O)
Cab-3f-3f-80	Adapter cable SMB female to SMB female, 80 cm (for clock and trigger I/O)
Cab-3f-9m-200	Adapter cable SMB female to BNC male, 200 cm (for clock and trigger I/O)
Cab-3f-9f-200	Adapter cable SMB female to BNC female, 200 cm (for clock and trigger I/O)
Cab-3f-3f-200	Adapter cable SMB female to SMB female, 200 cm (for clock and trigger I/O)

Drivers

Order no.	Option
UF/UC/UX-ml	MATLAB driver for all UF/UC/UX cards
UC.4600-lv	LabVIEW driver for all UC.4600 cards
UC.4600-dl	DASYLab driver for all UC.4600 cards
UC.4600-vee	Agilent VEE driver for all UC.4600 cards

(1) : Only one of the options can be installed on a card at a time.

technical changes and printing errors possible

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