UC.6000 : 14 bit 125 MS/s Arbitrary Waveform Generator

- **CompactPCI 6U format**
- **Fast 14 bit arbitrary waveform generators**
- **Models with 20 MS/s, 60 MS/s or 125 MS/s**
- **1, 2 or 4 channel versions**
- **Simultaneous sampling on all channels**
- **Output up to ± 3 V in 50 Ohm**
- **Amplifier option available for ±10 V**
- **Offset and amplitude programmable**
- **3 software selectable filters**
- **Up to 256 MSample memory**
- **FIFO mode**
- **Multiple card synchronization possible**
- **Bank Switching mode**
- **Software SPEasyGenerator included**

Product range overview

Model	1 channel	2 channels	4 channels
UC.6011	20 MS/s	20 MS/s	
UC.6012	20 MS/s	20 MS/s	20 MS/s
UC.6021	60 MS/s	60 MS/s	
UC.6022	60 MS/s	60 MS/s	60 MS/s
UC.6030	125 MS/s		
UC.6031	125 MS/s	125 MS/s	
UC.6033	125 MS/s	60 MS/s	
UC.6034	125 MS/s	125 MS/s	60 MS/s

Software/Drivers

A large number of drivers and examples are delivered with the board or are available as an option:

- Windows 98/ME/NT/2000/XP - drivers
- Linux - drivers
- SBench 5.2
- Microsoft Visual C++ examples
- Borland Delphi examples
- Microsoft Visual Basic examples
- Microsoft Excel examples
- LabWindows/CVI examples
- FlexPro support with SBench
- LabVIEW - drivers (as option)
- DASYLab - drivers (as option)
- MATLAB - drivers (as option)
- Agilent VEE - drivers (as option)

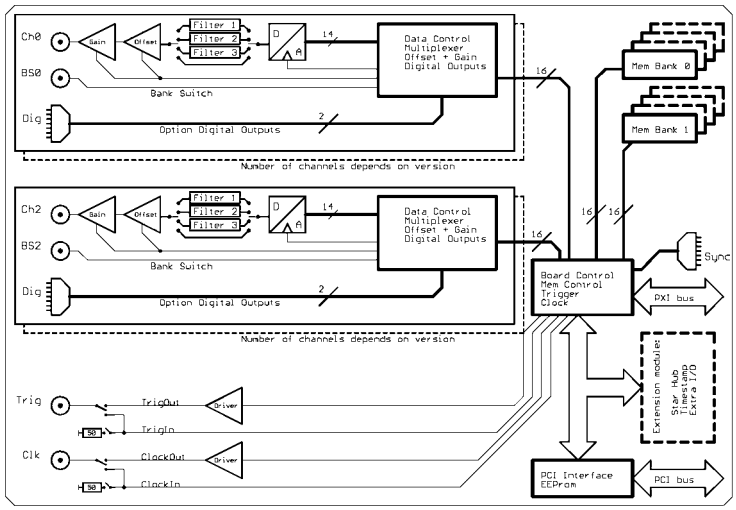
General Information

There are eight UC.6000 AWG cPCI cards with a choice of maximum output rates and either 1, 2 or 4 channels. With these boards it is possible to generate freely definable waveforms on multiple channels synchronously. Each channel has it's own 14-bit D/A and three software selectable reconstruction filters.

The internal standard Sync-bus allows multiple cards to be configured for higher chanel counts. It is also possible to combine the arbitrary waveform generator with other boards of the UC product family like analogue or digital boards.

With the up to 256 MSample on-board memory long waveforms can be generated even with high sampling rates. The memory can be used also as a FIFO buffer to make continuous data transfer from PC memory or hard disk.

Hardware block diagram



Software programmable parameters

Sampling rate	1 kS/s to max sampling rate, external clock, ref clock
Output amplitude	±100 mV up to ±3 V in 1 mV steps (Amp option: ±333 mV up to ±10 V)
Output offset	±3 V selectable in 1 mV steps (Amp otpion: ±10 V in 3 mV steps)
Filters	no filter or one of 3 different filters as defined in technical data section
Mode	Singleshot, Continuous, Standard, Bank Switching
Clock mode	internal PLL, int.quartz, external, ext. divided, ext. reference clock
Clock impedance	50 Ohm / 1 MOhm
Trigger impedance	50 Ohm / 1 MOhm
Trigger mode	External, Software
Memory depth	32 up to installed memory in steps of 32
Posttrigger	32 up to 128 M in steps of 32
Output amplitude	±100 mV up to ±3 V in 1 mV steps
Multiple Replay segmentsize	32 up to installed memory / 2 in steps of 32

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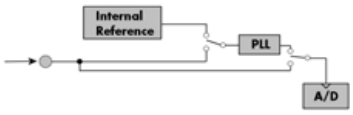
Possibilities and options

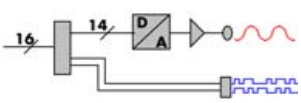
FIFO mode
The FIFO mode is designed for continuous data transfer between measurement board and PC memory (up to 100 MB /s) or hard disk (up to 50 MB/s). The control of the data stream is done automatically by the driver on interrupt request.

External trigger I/O
All boards can be triggered using an external TTL signal. It's possible to use positive or negative edge also in combination with a programmable pulse width. A softwate trigger event can, when activated by software, be routed to the trigger connector to start external instruments.

External clock I/O
Using a dedicated connector a sampling clock can be fed in from an external system. It's also possible to output the internal sampling clock to synchronise external equipment to this clock.

Reference clock


The option to use a precise external reference clock (normally 10 MHz) is necessary to synchronise the board for high-quality measurements with external equipment (like a signal source). It's also possible to enhance the quality of the sampling clock in this way. The driver automatically generates the requested sampling clock from the fed in reference clock.

Digital outputs


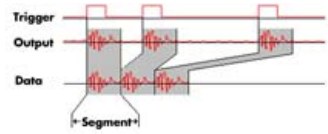
This option adds synchronous digital channels that are phase-stable analog data. When this option is installed there are 2 additional digital outputs for every analog D/A channel.

Bank Switching
In bank switching mode two different signals of the same length are written in the on-board memory. Controlled by an external bank signal that is individually available for every channel, one of the signals is selected for output. The user can define whether the signal should switch immediately or whether the complete signal should be generated up to the end.

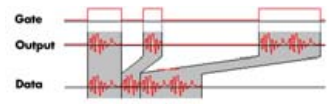
Cascading
The Cascading option synchronises up to 4 Strategic Test boards internally. It's the easiest way to build up a multi channel system. There is a phase delay between two boards of about 500 pico seconds when this synchronisation option is used.

Star Hub
The Star Hub is an additional module allowing the phase stable synchronisation of up to 16 boards. Independent of the number of boards there is no phase delay between all channels. The Star Hub distributes trigger and clock information between all boards. As a result all connected boards are running with the same clock and the same trigger.

Extra I/O
The Extra I/O module adds 24 additional digital I/O lines and 4 analog outputs on an extra connector. These additional lines are independent from the standard function and can be controlled asynchronously. There is also an internal version available with 16 digital I/Os and 4 analog outputs that can be used directly at the rear board connector.

Multiple Replay


The Multiple Replay option allows the fast repetition output on several trigger events without restarting the hardware. With this option very fast repetition rates can be achieved. The on-board memory is divided in several segments of same size. Each of them is generated if a trigger event occurs.

Gated Replay


The Gated Replay option allows signal generation controlled by an external gate signal. Data is only output if the gate signal has a programmed level.

Singleshot output
When singleshot output is activated the data in the on-board memory is output exactly one time. Either the external TTL trigger or the software trigger can be used.

Continuous output
When continuous output is activated the data of the on-board memory is replayed continuously until a stop command is executed. As trigger source one can use the external TTL trigger or the software trigger.

±10 V Amplifier

The amplifier board allows the output of ±10 V on up to four channels without software modification. The standard outputs of the card are amplified by factor 3.33. The amplifier has a 30 MHz bandwidth and an output impedance of 50 Ohm. This allows ±10 V with high impedance termination or ±5 V with 50 Ohm termination.

Technical Data

Resolution (UC.6000)	14 bit	Dimension	160 mm x 233 mm (Standard 6U)
Integral linearity (DAC)	± 1.5 LSB typ.	Width (Standard)	1 slot (6U)
Differential linearity (DAC)	± 1.0 LSB typ.	Width (with digital outputs)	2 slots (6U)
Output resistance	< 1 Ohm	Width (with star hub option)	2 slots (6U)
Max output swing in 50 Ohm	± 3 V (offset + amplitude)	Width of Amplifier option	1 slot (3U)
Max slew rate (no filter)	> 0.9 V/ns	Analogue connector	3 mm SMB male
Multi: Trigger to 1st sample delay	fixed	Digital connector	40 pol half pitch (Hirose FX2 series)
Multi: Recovery time	< 20 samples	Digital Outputs delay to analog sample	0 samples (due to internal correction)
Ext. clock: delay to internal clock	42 ns ± 2 ns	Warm up time	10 minutes
Output to trigger out delay 1 channel	< 5 MS/s: -5 samples, > 5 MS/s: -21 samples	Operating temperature	0°C - 50°C
Output to trigger out delay 2 channels	< 5 MS/s: -3.5 samples, > 5 MS/s: -12 sampl.	Storage temperature	-10°C - 70°C
Crosstalk @ 1 MHz signal ±3 V	< -80 dB	Humidity	10% to 90%
Output accuracy	< 1%	Offset stepsize	< 2 mV
Min internal clock	1 kS/s	Amplitude stepsize	< 1 mV
Min external clock	DC	Power consumption 3.3 V @ full speed	max. 1.51 A (5.0Watt)
		Power consumption 5 V @ full speed	max. 1.53 A (7.7 Watt)
Trigger input:Standard TTL level	Low: -0.5 > level < 0.8 V High: 2.0 V > level < 5.5 V Trigger pulse must be valid ≥ 2 clock periods.	Clock input: Standard TTL level	Low: -0.5 V > level < 0.8 V High: 2.0 V > level < 5.5 V Rising edge. Duty cycle: 50% ± 5%
Trigger output	Standard TTL, capable of driving 50 Ohm. Low < 0.4 V (@ 20 mA, max 64 mA) High > 2.4 V (@ -20 mA, max -48 mA) One positive edge after the first internal trigger	Clock output	Standard TTL, capable of driving 50 Ohm Low < 0.4 V (@ 20 mA, max 64 mA) High > 2.4 V (@ -20 mA, max -48 mA)

Clock and Filter

	UC.6011 UC.6012	UC.6021 UC.6022	UC.6030 UC.6033	UC.6031 UC.6034
max internal clock	20 MS/s	60 MS/s	125 MS/s	125 MS/s
max external clock	20 MS/s	60 MS/s	125 MS/s	125 MS/s
-3 dB bandwidth no filter	> 10 MHz	> 30 MHz	> 60 MHz	> 60 MHz
Filter 3: Characteristics	4th order Butterworth		5th order Butterworth	
Filter 3: -3 dB bandwidth	5 MHz	10 MHz	25 MHz	25 MHz
Filter 2: Characteristics	4th order Butterworth		4th order Butterworth	
Filter 2: -3 dB bandwidth	1 MHz	2 MHz	5 MHz	5 MHz
Filter 1: Characteristics	4th order Butterworth		4th order Butterworth	
Filter 1: -3 dB bandwidth	100 kHz	200 kHz	500 kHz	500 kHz

Dynamic Parameters

	UC.6011 UC.6012	UC.6011 UC.6012	UC.6011 UC.6012	UC.6021 UC.6022	UC.6021 UC.6022	UC.6030 UC.6031 UC.6033 UC.6034	UC.6030 UC.6031 UC.6033 UC.6034	UC.6030 UC.6031 UC.6033 UC.6034	UC.6030 UC.6031 UC.6033 UC.6034
Test - Sample rate	20 MS/s	20 MS/s	20 MS/s	60 MS/s	60 MS/s	62.5 MS/s	62.5 MS/s	125 MS/s	125 MS/s
Output Frequency	80 kHz	800 kHz	4 MHz	170 kHz	1.7 MHz	400 kHz	4 MHz	400 kHz	4 MHz
Output Level	±2 V	±2 V	±2 V	±2 V	±2 V	±2 V	±2 V	±2 V	±2 V
Used Filter	100 kHz	1 MHz	5 MHz	200 kHz	2 MHz	500 kHz	5 MHz	500 kHz	5 MHz
SNR (typ)	> 61.5 dB	> 60.2 dB	> 54.5 dB	> 61.5 dB	> 59.5 dB	> 61.2 dB	> 54.5 dB	> 60.2 dB	> 55.0 dB
THD (typ)	< -70.4 dB	< -67.5 dB	< -45.0 dB	< -72.7 dB	< -62.5 dB	< -71.5 dB	< -55.6 dB	< -71.5 dB	< -56.0 dB
SFDR (typ), excl harm.	> 85.5 dB	> 72.0 dB	> 60.0 dB	> 81.5 dB	> 68.5 dB	> 81.5 dB	> 65.5 dB	> 71.0 dB	> 66.0 dB

Dynamic parameters are measured at the given output level and 50 Ohm termination with a high resolution data acquisition card and are calculated from the spectrum. The sample rate that is selected is the maximum possible one. All available channels are activated for the tests. SNR and SFDR figures may differ depending on the quality of the used PC. SNR = Signal to Noise Ratio, THD = Total Harmonic Distortion, SFDR = Spurious Free Dynamic Range

Order information

Order No	Description	Order No	Description
UC6011	UC.6011 with 8 MSample memory and drivers/SBench 5.x	UC6000-16M	Option: 16 MSample memory instead of 8 MSample standard mem
UC6012	UC.6012 with 8 MSample memory and drivers/SBench 5.x	UC6000-32M	Option: 32 MSample memory instead of 8 MSample standard mem
UC6021	UC.6021 with 8 MSample memory and drivers/SBench 5.x	UC6000-64M	Option: 64 MSample memory instead of 8 MSample standard mem
UC6022	UC.6022 with 8 MSample memory and drivers/SBench 5.x	UC6000-128M	Option: 128 MSample memory instead of 8 MSample standard mem
UC6030	UC.6030 with 8 MSample memory and drivers/SBench 5.x	UC6000-256M	Option: 256 MSample memory instead of 8 MSample standard mem
UC6031	UC.6031 with 8 MSample memory and drivers/SBench 5.x	UC6000-up	Additional handling cost for later memory upgrade
UC6033	UC.6033 with 8 MSample memory and drivers/SBench 5.x		
UC6034	UC.6034 with 8 MSample memory and drivers/SBench 5.x	UC6000-smod	Star Hub: Synchronisation of 2 - 16 boards, one option per system
		UC6000-xmf	Extra I/O, external connector: 24 DI/O, 4 Analog out, incl. cable
UC6000-mr	Option Multiple Replay: Memory segemntation		
UC6000-gs	Option Gated Sampling: Gate signal controls replay	MC6000-1Amp	±10 V Amplifier board with 1 channel
UC6000-dig	Additional 2 synchronous digital outputs per channel, incl. cable	MC6000-2Amp	±10 V Amplifier board with 2 channels
UC6000-cs	Synchronisation of 2 - 4 boards, one option per system	MC6000-4Amp	±10 V Amplifier board with 4 channels
Cab-3f-9m-80	Adapter cable: SMB female to BNC male 80 cm	UC6000-dl	DASYLab driver for UC.6000 series
Cab-3f-9m-200	Adapter cable: SMB female to BNC male 200 cm	UC6000-hp	VEE driver for UC.6000 series
Cab-3f-9f-80	Adapter cable: SMB female to BNC female 80 cm	UC6000-lv	LabVIEW driver for UC.6000 series
Cab-3f-9f-200	Adapter cable: SMB female to BNC female 200 cm	UF/UC/UX-ml	MATLAB driver for all UF/UC/UX series.

technical changes and printing errors possible