UltraFast

UC.7000 : 64 bit High-Speed Digital I/O cards, TTL levels

- **CompactPCI 6U format**
- **1, 2, 4, 8 or16 bit, 32 bit or 64 bit digital I/O**
- **1 kS/s up to 125 MS/s at 16 and 32 bit**
- **1 kS/s up to 60 MS/s at 32 and 64 bit**
- **110 Ohm input impedance selectable**
- **Inputs 3.3 V and 5 V TTL compatible**
- **Outputs 3.3 V TTL compatible**
- **Up to 512 MByte memory**
- **FIFO mode for input and output**
- **Pattern/Edge/Pulsewidth trigger**
- **Multiple card synchronization option**
- **Windows program SBench 5.x included**

Product range overview

Model	1-4 bit	8 bit	16 bit	32 bit	64 bit
UC.7005	125 MS/s	125 MS/s	125 MS/s		
UC.7010		125 MS/s	125 MS/s		
UC.7011		125 MS/s	125 MS/s	60 MS/s	
UC.7020		125 MS/s	125 MS/s	125 MS/s	
UC.7021		125 MS/s	125 MS/s	125 MS/s	60 MS/s

Software/Drivers

A large number of drivers and examples are delivered with the board or are available as an option:

- Windows 98/ME/NT/2000/XP - drivers
- Linux - drivers
- SBench 5.2
- Streaming Software SPviewIT 6.1(as option, recording only)
- Microsoft Visual C++ examples
- Borland Delphi examples
- Microsoft Visual Basic examples
- Microsoft Excel examples
- LabWindows/CVI examples
- FlexPro support with SBench
- LabVIEW - drivers (as option)
- DASYLab - drivers (as option)
- MATLAB - drivers (as option)
- Agilent VEE - drivers (as option)

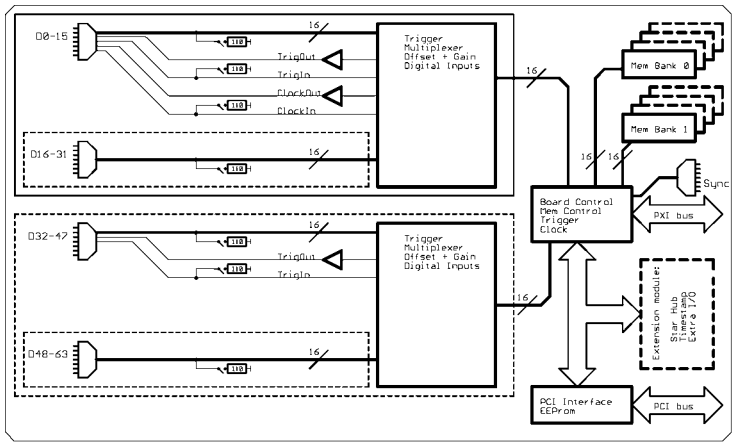
General Information

The UC.7000 series of high-speed digital I/O boards offer a resolution between 1 bit and 64 bit with a maximum sampling rate of 125 MS/s (60 MS/s). Every 16 bit / 32 bit of the board can be separately programmed for input or output.

The on-board memory of up to 512 MByte can be completely used for recording or replaying digital data. Alternatively the UC.7000 can be used in FIFO mode. Then data is transferred on-line to PC memory or hard disk.

The internal standard synchronisation bus allows synchronisation of several UC boards, even of different types to create mixed signal test systems.

Hardware block diagram



Software programmable parameters

sampling rate	1 kS/s to max sampling rate, external clock, ref clock
Direction	Input/Output for each module
Input impedance	110 Ohm / 50 kOhm for each channel
Clock mode	internal PLL, int.quartz, external, ext. divided, ext. reference clock
Clock impedance	110 Ohm / 50 kOhm
Trigger impedance	110 Ohm / 50 kOhm
Trigger pulsewidth	1 to 256 sanples in steps of 1
Trigger mode	Pattern and mask, edge, external TTL, software
Pattern and mask	32 bit / 64 bit wide: 0 pattern, 1 patterm, don't care or edge
Memory depth	32 up to installed memory in steps of 32
Posttrigger	32 up to 128 M in steps of 32
Multiple Replay segmentsize	32 up to installed memory / 2 in steps of 32

Application examples

Semiconductor test	Production test	Pattern generator
A/D data acquisition	Logic analyser	Pattern recognition

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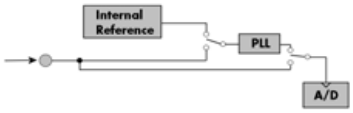
Possibilities and options

FIFO mode
The FIFO mode is designed for continuous data transfer between measurement board and PC memory (up to 100 MB /s) or hard disk (up to 50 MB/s). The control of the data stream is done automatically by the driver on interrupt request.

Pattern trigger
For every bit of the digital input the pattern trigger defines individually the expected level or sets the bit to "don't care". In combination with pulsewidth counter and edge detection the pattern trigger can be used to recognise a wide variety of trigger events.

External trigger I/O
All boards can be triggered using an external TTL signal. It's possible to use positive or negative edge also in combination with a programmable pulse width. A softwate trigger event can, when activated by software, be routed to the trigger connector to start external instruments.

External clock I/O
Using a dedicated connector a sampling clock can be fed in from an external system. It's also possible to output the internal sampling clock to synchronise external equipment to this clock.

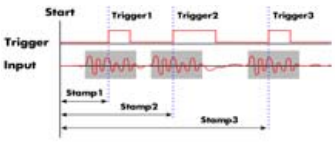
Reference clock


The option to use a precise external reference clock (normally 10 MHz) is necessary to synchronise the board for high-quality measurements with external equipment (like a signal source). It's also possible to enhance the quality of the sampling clock in this way. The driver automatically generates the requested sampling clock from the fed in reference clock.

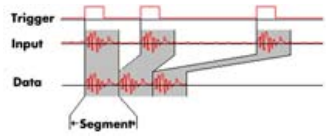
Cascading
The Cascading option synchronises up to 4 Strategic Test boards internally. It's the easiest way to build up a multi channel system. There is a phase delay between two boards of about 500 pico seconds when this synchronisation option is used.

Star Hub
The Star Hub is an additional module allowing the phase stable synchronisation of up to 16 boards. Independent of the number of boards there is no phase delay between all channels. The Star Hub distributes trigger and clock information between all boards. As a result all connected boards are running with the same clock and the same trigger.

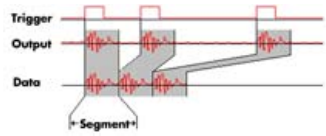
Extra I/O
The Extra I/O module adds 24 additional digital I/O lines and 4 analog outputs on an extra connector. These additional lines are independent from the standard function and can be controlled asynchronously. There is also an internal version available with 16 digital I/Os and 4 analog outputs that can be used directly at the rear board connector.

Timestamp


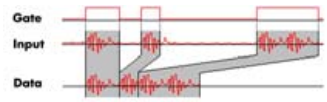
The timestamp option writes the time positions of the trigger events in an extra memory. The timestamps are relative to the start of recording, a defined zero time, externally synchronised to a radio clock, or a GPS receiver. With this option acquisitions of systems on different locations can be set in a precise time relation.

Multiple Recording


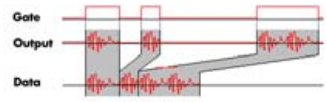
The Multiple Recording option allows the recording of several trigger events without restarting the hardware. This enables very fast repetition rates to be achieved. The on-board memory is divided in several segments of same size. Each of them is filled with data if a trigger event occurs.

Multiple Replay


The Multiple Replay option allows the fast repetition output on several trigger events without restarting the hardware. With this option very fast repetition rates can be achieved. The on-board memory is divided in several segments of same size. Each of them is generated if a trigger event occurs.

Gated Sampling


The Gated Sampling option allows data recording controlled by an external gate signal. Data is only recorded if the gate signal has a programmed level.

Gated Replay


The Gated Replay option allows signal generation controlled by an external gate signal. Data is only output if the gate signal has a programmed level.

Singleshot output
When singleshot output is activated the data in the on-board memory is output exactly one time. Either the external TTL trigger or the software trigger can be used.

Continuous output
When continuous output is activated the data of the on-board memory is replayed continuously until a stop command is executed. As trigger source one can use the external TTL trigger or the software trigger.

1-4 bits mode
On the 7005 model it is also possible to use only 1, 2 or 4 bits for acquisition or replay. In 1 bit mode 8 times more memory is then available, at 2 bits mode it is 4 times more and at 4 bits mode it is double. This enlarges the recording/replay time in on-board memory and it reduces the transfer rate when using FIFO mode. The data is stacked internally to 8 bit samples. Therefore all information on memory/segment/pre and posttrigger sizes and steps can be up to 8 times more.

Technical Data

Internal samplerate	1 kS/s up to 125 MS/s						
External samplerate	DC up to 125 MS/s						
Input impedance	110 Ohm / 50 kOhm || 15 pF						
110 Ohm termination voltage	2.5V						
Signal level (data, trigger, clock)	3.3 V/ 5 V TTL compatible						
	LOW		HIGH				
Data input current sink (no termination)	0.0 V -1.0 µA	3.3 V +1.0 µA	5.0 V +20.0 µA				
Clock / trigger input current sink (no termination)	± 1.0 µA						
Multi: Trigger to 1st sample delay	fixed						
Multi: Recovery time	< 20 samples (16 - 64 bit)						

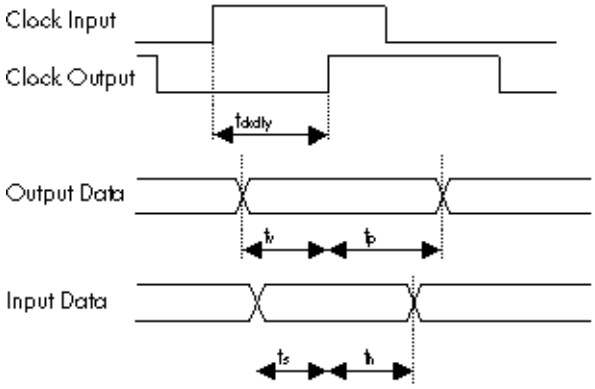
	64 bit	32 bit	16 bit	8 bit	4 bit	2 bit	1 bit
ext. Trigger accuracy (samples)	1	1	1	2	4	8	16
int. Trigger accuracy (samples)	1	1	1	2	4	8	16

Trigger input:Standard TTL level	Low: -0.5 > level < 0.8 V High: 2.0 V > level < 5.5 V Trigger pulse must be valid ≥ 2 clock periods.	Clock input: Standard TTL level	Low: -0.5 V > level < 0.8 V High: 2.0 V > level < 5.5 V Rising edge. Duty cycle: 50% ± 5%
Trigger output	Standard TTL, capable of driving 50 Ohm. Low < 0.4 V (@ 20 mA, max 64 mA) High > 2.4 V (@ -20 mA, max -48 mA) One positive edge after the first internal trigger	Clock output	Standard TTL, capable of driving 50 Ohm Low < 0.4 V (@ 20 mA, max 64 mA) High > 2.4 V (@ -20 mA, max -48 mA)

Power consumption (maximum value)			Full speed	
	+3,3 V	+5 V	+12 V	-12 V
UC.7005 (16 bit output @ 125 MS/s in 110 Ohm)	1.25 A (4.2 W)	0.91 A (4.6 W)	0 A	0 A
UC.7010 (16 bit output @ 125 MS/s in 110 Ohm)	1.25 A (4.2 W)	0.91 A (4.6 W)	0 A	0 A
UC.7011 (32 bit output @ 60 MS/s in 110 Ohm)	1.77 A (5.8 W)	0.91 A (4.6 W)	0 A	0 A
UC.7020 (32 bit output @ 125 MS/s in 110 Ohm)	2.29 A (7.6 W)	1.30 A (6.5 W)	0 A	0 A
UC.7021 (64 bit output @ 60 MS/s in 110 Ohm)	2.31 A (7.6 W)	1.27 A (6.4 W)	0 A	0 A

For detailed information on the different modes for external clocking please refer to the dedicated chapter in the 7000 series hardware manual.

	External Clocking Mode		
Delay time	SINGLE	BURST_S	BURST_M
t_{ckdly}	20 ns	30 ns	< 1 ns
t_v	> 350 ns	> 150 ns	> 2.5 ns
t_p	> 2.5 ns	> 2.5 ns	> 2.5 ns
t_s	≤ 3.0 ns	≤ 3.0 ns	≤ 3.0 ns
t_{Vh}	≤ 1.0 ns	≤ 1.0 ns	≤ 1.0 ns



Order information

Order No	Description	Order No	Description
UC7005	UC.7005 with 16 MByte (128 MBit) memory, cables and drivers	UC7000-32M	Option: 32 MByte memory instead of 16 MByte standard mem
UC7010	UC.7010 with 16 MByte (128 MBit) memory, cables and drivers	UC7000-64M	Option: 64 MByte memory instead of 16 MByte standard mem
UC7011	UC.7011 with 16 MByte (128 MBit) memory, cables and drivers	UC7000-128M	Option: 128 MByte memory instead of 16 MByte standard mem
UC7020	UC.7020 with 16 MByte (128 MBit) memory, cables and drivers	UC7000-256M	Option: 256 MByte memory instead of 16 MByte standard mem
UC7021	UC.7021 with 16 MByte (128 MBit) memory, cables and drivers	UC7000-512M	Option: 512 MByte memory instead of 16 MByte standard mem
		UC7000-up	Additional handling costs for later memory upgrade
UC7000-smod	Star Hub: Synchronisation of 2 - 16 boards, one option per system		
UC7000-time	Timestamp option: Extra memory for trigger time	UC7000-mr	Option Multiple Recording/Replay: Memory segmentation
UC7000-xmf	Extra I/O, external connector: 24 DI/O, 4 Analog out, incl. cable	UC7000-gs	Option Gated Sampling: Gate signal controls acquisition/replay
		UC7000-cs	Synchronisation of 2 - 4 boards, one option per system
UC7000-dl	DASYLab driver for UC.7000 series		
UC7000-hp	VEE driver for UC.7000 series		
UC7000-lv	LabVIEW driver for UC.7000 series	UC7000-dcab	Additional 40 pole flat ribbon cable with IDC socket connector, 1 m
UF/UC/UX-ml	MATLAB driver for all UF/UC/UX series.	UC7000-dcab2	Additional 40 pole flat ribbon cable withFx2 connector, ca. 1 m

technical changes and printing errors possible