UC.7200 : 32 bit Digital Pattern Generators with programmable logic levels

- **CompactPCI 6U format**
- **Programmable output levels from -2,0 V up to +10,0 V**
- **Levels individually programmable per 4 bit**
- **Up to 40 MS/s at 32 bit**
- **Possible use of memory saving 8 bit mode**
- **All outputs can be separately disabled (Tristate)**
- **Hardware controlled differential output possible (8 bit and 16 bit)**
- **Up to 512 MByte on-board memory**
- **Output in FIFO mode**
- **Multiple card synchronization option**

Product range overview

Model	8 bit	16 bit	32 bit
UC.7210	10 MS/s	10 MS/s	
UC.7211	10 MS/s	10 MS/s	5 MS/s
UC.7220	40 MS/s	40 MS/s	
UC.7221	40 MS/s	40 MS/s	40 MS/s

Software/Drivers

A large number of drivers and examples are delivered with the board or are available as an option:

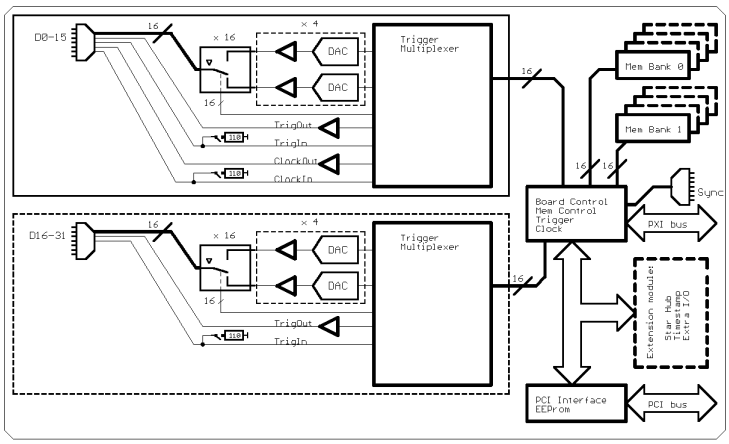
- Windows 98/ME/NT/2000/XP - drivers
- Linux - drivers
- SBench 5.2
- Microsoft Visual C++ examples
- Borland Delphi examples
- Microsoft Visual Basic examples
- Microsoft Excel examples
- LabWindows/CVI examples
- FlexPro support with SBench
- LabVIEW - drivers (as option)
- DASYLab - drivers (as option)
- MATLAB - drivers (as option)
- Agilent VEE - drivers (as option)

General Information

The UC.7200 pattern generator series gives the user the possibility to generate digital data with a wide range of output levels. For every 4 bit the LOW and HIGH levels can be programmed from -2.0 V up to +10.0 V. Even at high speeds you are not limited concerning the maximum output swing. This enables the user to drive devices of nearly any logic family, like ECL, PECL, TTL, LVDS, LVTTL, CMOS or LVCMOS. The potentially necessary differential signals are generated in hardware, so that only one data bit is used for each pair of differential signals. All outputs can be seperately disabled allowing the easy connection with digital acquisition boards and the adaption to a wide range of test setups.

With up to 512 MBytes memory long waveforms can be generated even with high sampling rates. The memory can also be used as a FIFO buffer for continuous data transfer from PC memory or hard disk.

Hardware block diagram



Software programmable parameters

Sampling rate	1 kS/s to max sampling rate, external clock, ref clock
Output level	LOW/HIGH level p. nibble;-2,0 V up to +10,0 V in steps of 1mV
Clock mode	internal PLL, int.quartz, external, ext. divided, ext. reference clock
Clock impedance	110 Ohm / 50 kOhm
Trigger impedance	110 Ohm / 50 kOhm
Data Enable mask	programmable for every single bit
Trigger mode	External TTL, software
Memory depth	32 up to installed memory in steps of 32
Posttrigger	32 up to 256 M in steps of 32
Multiple Recording segmentsize	32 up to installed memory / 2 in steps of 32

Application examples

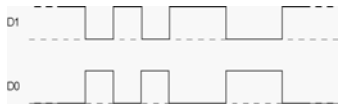
Semiconductor test	Production test	Burn-in test
Laboratory purposes	Pattern generator	Semiconductor development
Process control	ATE	

Possibilities and options

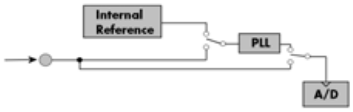
FIFO mode
The FIFO mode is designed for continuous data transfer between measurement board and PC memory (up to 100 MB /s) or hard disk (up to 50 MB/s). The control of the data stream is done automatically by the driver on interrupt request.

External trigger I/O
All boards could be triggered using an external TTL signal. It's possible to use positive or negative edge. An internally recognised trigger event could - activated by software - routed to the output connector to start external instruments.

External clock I/O
Using a dedicated connector a sampling clock can be fed in from an external system. It's also possible to output the internal sampling clock to synchronise external equipment to this clock.

ECL Mode


When the ECL mode is activated, differential signals wich are needed for e.g. ECL interfacing are generated in hardware on the odd data outputs. This results in the use of only one data bit for every pair of differential outputs and allows a very efficiently use of memory.

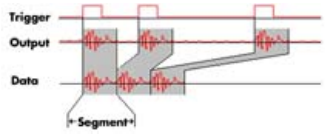
Reference clock


The option to use a precise external reference clock (normally 10 MHz) is necessary to synchronise the board for high-quality measurements with external equipment (like a signal source). It's also possible to enhance the quality of the sampling clock in this way. The driver automatically generates the requested sampling clock from the fed in reference clock.

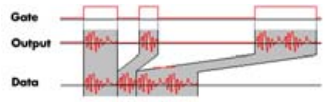
Cascading
The Cascading option synchronises up to 4 Strategic Test boards internally. It's the easiest way to build up a multi channel system. There is a phase delay between two boards of about 500 pico seconds when this synchronisation option is used.

Star Hub
The Star Hub is an additional module allowing the phase stable synchronisation of up to 16 boards. Independent of the number of boards there is no phase delay between all channels. The Star Hub distributes trigger and clock information between all boards. As a result all connected boards are running with the same clock and the same trigger.

Extra I/O
The Extra I/O module adds 24 additional digital I/O lines and 4 analog outputs on an extra connector. These additional lines are independent from the standard function and can be controlled asynchronously. There is also an internal version available with 16 digital I/Os and 4 analog outputs that can be used directly at the rear board connector.

Multiple Replay


The Multiple Replay option allows the fast repetition output on several trigger events without restarting the hardware. With this option very fast repetition rates can be achieved. The on-board memory is divided in several segments of same size. Each of them is generated if a trigger event occurs.

Gated Replay


The Gated Replay option allows signal generation controlled by an external gate signal. Data is only output if the gate signal has a programmed level.

Singleshot output
When singleshot output is activated the data in the on-board memory is output exactly one time. Either the external TTL trigger or the software trigger can be used.

Continuous output
When continuous output is activated the data of the on-board memory is replayed continuously until a stop command is executed. As trigger source one can use the external TTL trigger or the software trigger.

Technical Data

Internal samplerate	1 kS/s up to maximum (depending on model)			Dimension	160 mm x 233 mm (Standard 6U)
External samplerate	DC up to maximum (depending on model)			Width (UC.721x)	1 slot
Clock input impedance	110 Ohm / 50 kOhm || 15 pF			Width (UC.722x)	2 slots
Trigger input impedance	110 Ohm / 50 kOhm || 15 pF				
Output impedance	approximately 80 Ohm			Output connector	40 pole half pitch (Hirose FX2 series)
Data signal level	programmable from -2.0 V up to +10.0 V with an accuracy of ±10 mV			Power connector (UC.722x only)	soldered Y - cable with Molex 8981 (5,25" disc drive connector)
Output swing	0.1 ... 12.0 V				
	per pin	per nibble	per card	Operating temperature	0°C to 50°C
Maxixmum output current	100 mA	200 mA	0.5 A (UC.721x only)	Storage temperature	-10°C to 70°C
	1 MHz	40 MHz		Humidity	10% to 90%
Rise time[a]	2.00 ns	2.25 ns			
Fall time[a]	2.00 ns	2.25 ns			
Multi: Trigger to 1st sample delay	fixed				
Multi: Recovery time	< 20 samples (16 - 32 bit)				
	32 bit	16 bit	8 bit		
Trigger accuracy (samples)	1	1	2		

a. Tested with full output swing from -2.0 V to 10.0 V with no load

Trigger input:Standard TTL level	Low: -0.5 > level < 0.8 V High: 2.0 V > level < 5.5 V Trigger pulse must be valid ≥ 2 clock periods.	Clock input: Standard TTL level	Low: -0.5 V > level < 0.8 V High: 2.0 V > level < 5.5 V Rising edge. Duty cycle: 50% ± 5%
Trigger output	Standard TTL, capable of driving 50 Ohm. Low < 0.4 V (@ 20 mA, max 64 mA) High > 2.4 V (@ -20 mA, max -48 mA) One positive edge after the first internal trigger	Clock output	Standard TTL, capable of driving 50 Ohm Low < 0.4 V (@ 20 mA, max 64 mA) High > 2.4 V (@ -20 mA, max -48 mA)

Power consumption (maximum value)	Full speed			
	+3.3 V (CPCI Bus)	+5 V (CPCI Bus)	+12 V (CPCI Bus)	+12 V (Connector)
UC.7211 (32 bit output @ 5 MS/s)[a]	0.65 A (2.1 W)	0.61 A (3.1 W)	0.40 A (4.8 W)	0 A
UC.7221 (32 bit output @ 40 MS/s)[b]	1.07 A (3.5 W)	1.02 A (5.1 W)	0 A	3.6 A (43.2 W)

a. Tested with full output swing from -2.0 to 10.0 V with no load
b. Tested with full output swing from -2.0 V to 10.0 V with 50 mA output current per pin

Order information

Order No	Description	Order No	Description
UC7210	UC.7210 with 16 MByte (128 MBit) memory, cables and drivers	UC7000-32M	Option: 32 MByte memory instead of 16 MByte standard mem
UC7211	UC.7211 with 16 MByte (128 MBit) memory, cables and drivers	UC7000-64M	Option: 64 MByte memory instead of 16 MByte standard mem
UC7220	UC.7220 with 16 MByte (128 MBit) memory, cables and drivers	UC7000-128M	Option: 128 MByte memory instead of 16 MByte standard mem
UC7221	UC.7221 with 16 MByte (128 MBit) memory, cables and drivers	UC7000-256M	Option: 256 MByte memory instead of 16 MByte standard mem
		UC7000-512M	Option: 512 MByte memory instead of 16 MByte standard mem
UC7000-smod	Star Hub: Synchronisation of 2 - 16 boards, one option per system	UC7000-up	Additional handling cost for later memory upgrade
UC7200-xmf	Extra I/O, external connector: 24 DI/O, 4 Analog out, incl. cable	UC7000-mr	Option Multiple Replay: Memory segmentation
		UC7000-gs	Option Gated Replay: Gate signal controls replay
UC7200-dl	DASYLab driver for UC.7200 series	UC7000-cs	Synchronisation of 2 - 4 boards, one option per system
UC7200-hp	VEE driver for UC.7200 series		
UC7200-lv	LabVIEW driver for UC.7200 series	UC7200-dcab	Additional 40 pole flat ribbon cable with IDC socket connector, 1 m
UF/UC/UX-ml	MATLAB driver for all UF/UC/UX series.	UC7200-dcab2	Additional 40 pole flat ribbon cable withFx2 connector, ca. 1 m

technical changes and printing errors possible

STRATEGIC TEST
The High-Speed Specialists

STRATEGIC TEST CORPORATION · STOCKHOLM, SWEDEN · WOBURN, MA, USA
EUROPE PHONE: +46 (854)400-490 · USA PHONE: +1 (617)621-0080 · E-MAIL: info@strategic-test.com · INTERNET: http://www.strategic-test.com